HARDENING SECURE BOOT ON EMBEDDED DEVICES FOR HOSTILE ENVIRONMENTS

riscure

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PULSE

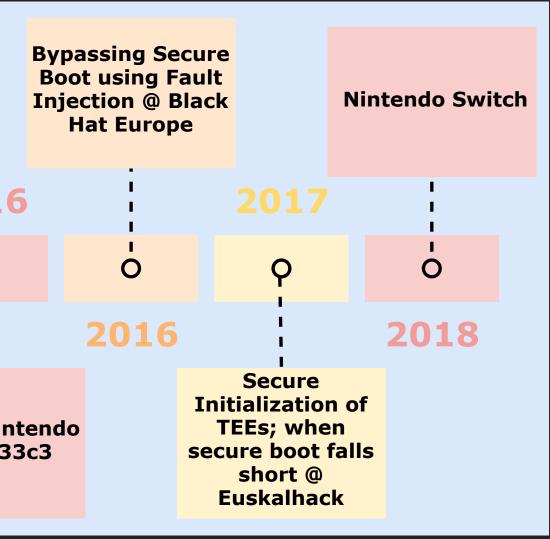
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WHY THIS TALK?

SOME HISTORY...

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SECURE BOOT IS STILL OFTEN VULNERABLE...

OUR GOAL

Create a <u>Secure Boot guidance</u> for designers, implementers and integrators.

WHITE PAPER

"Notes on Designing Secure Boot."

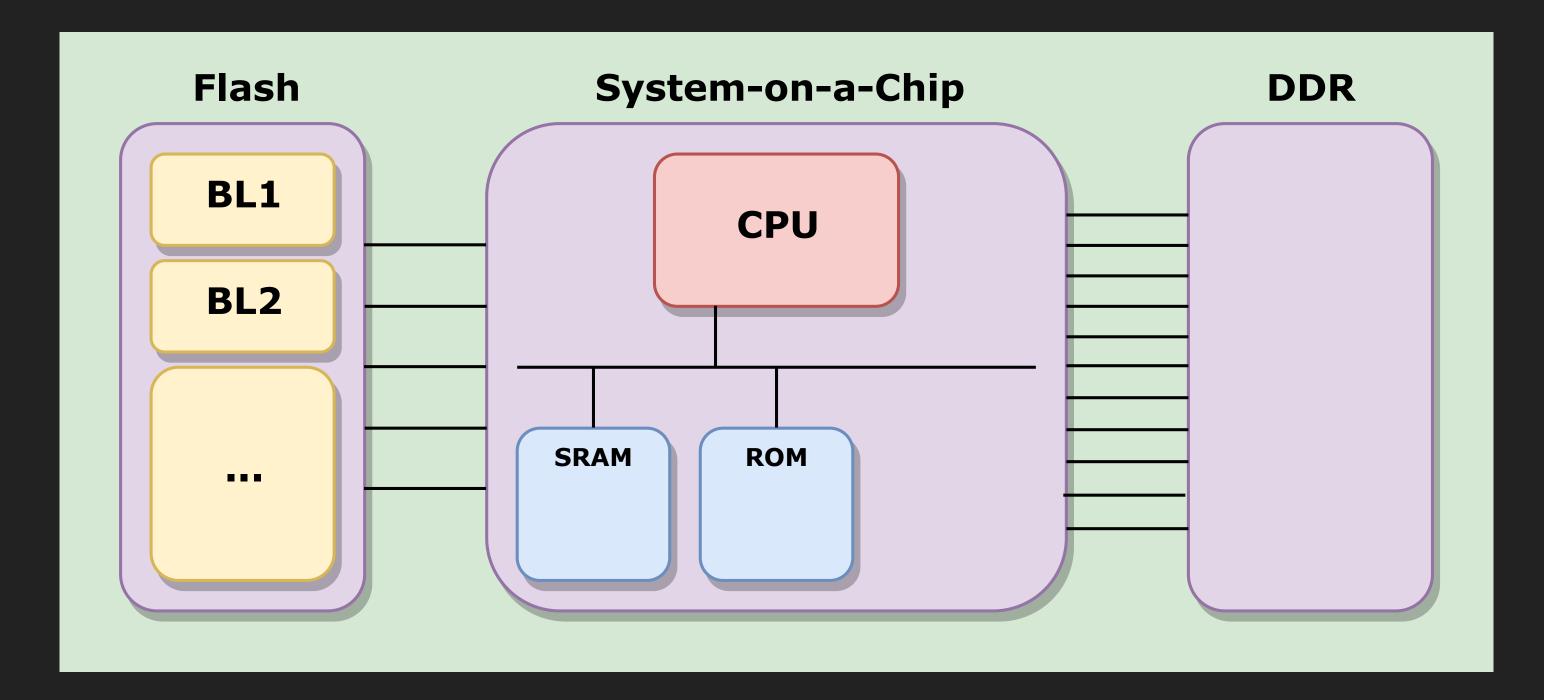
We are working on it!



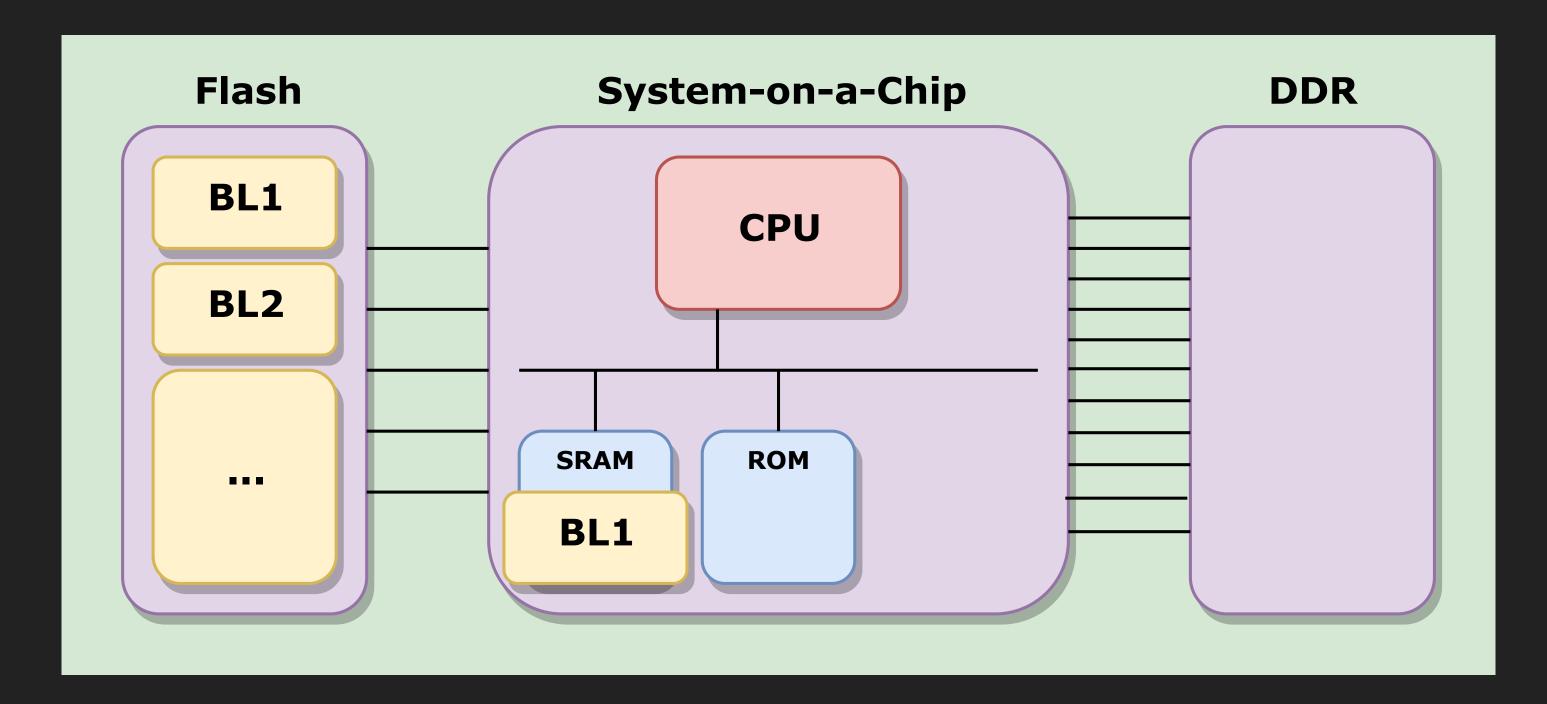
THIS PRESENTATION

Offensive focus Known and new attacks New perspectives

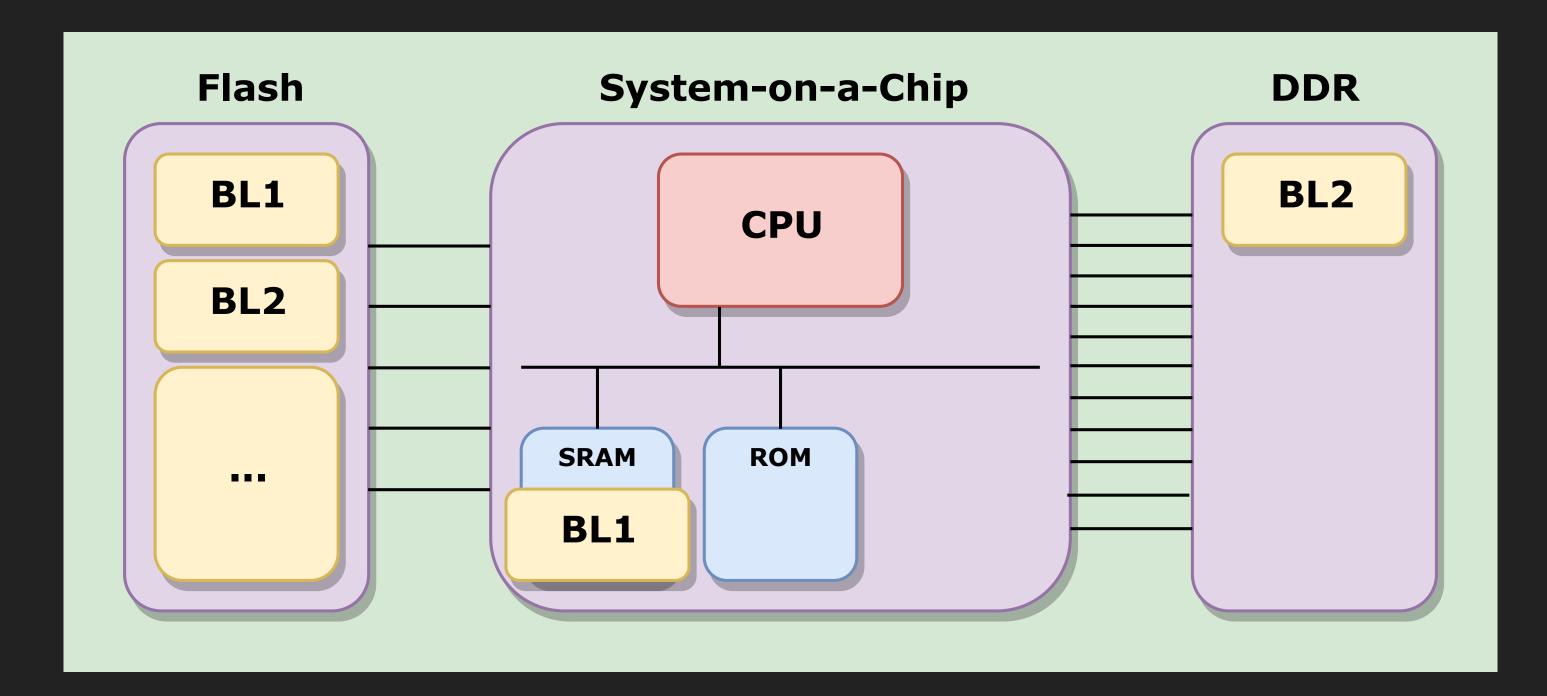
AGENDA Introduction Secure Boot Attacks and Mitigations Demo Takeaways



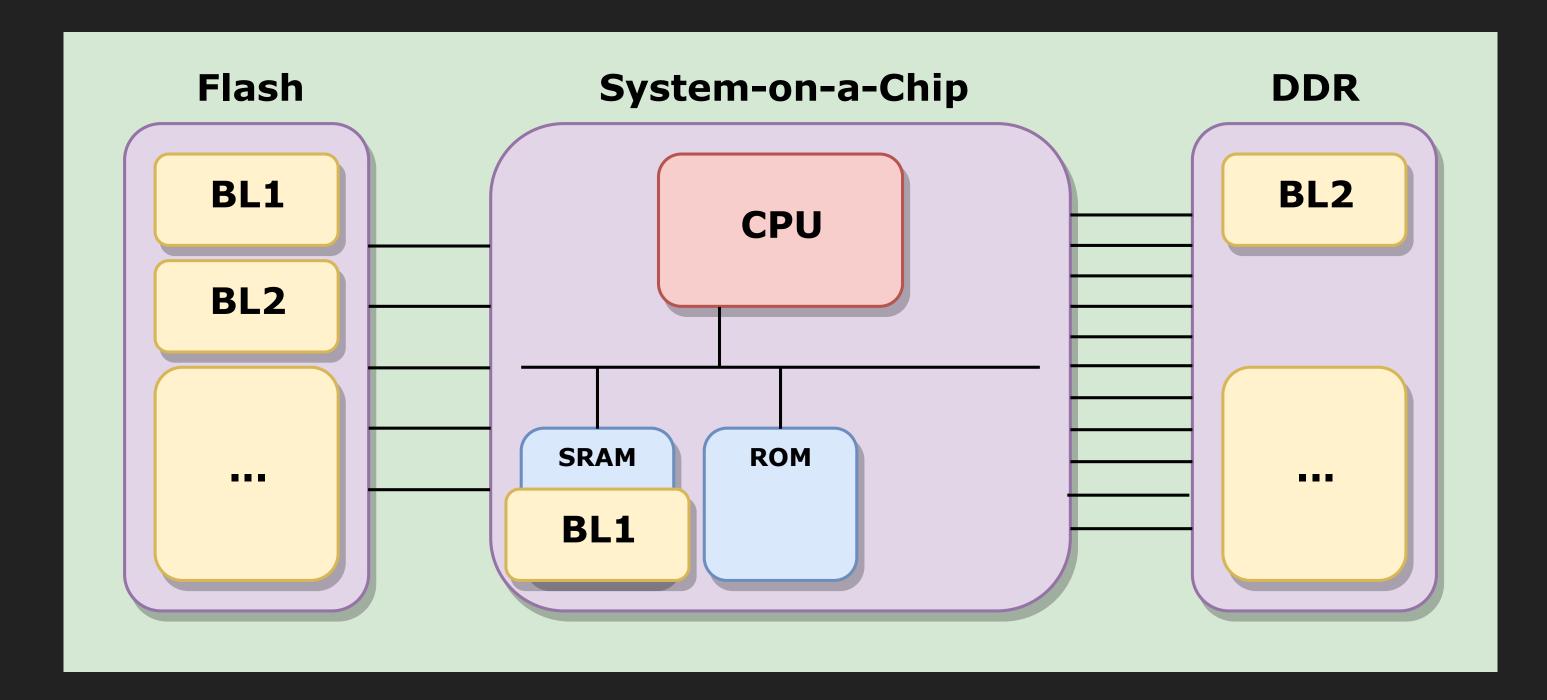
Device is turned off



ROM code loads BL1 into internal SRAM



BL1 initializes DDR and loads BL2 into DDR

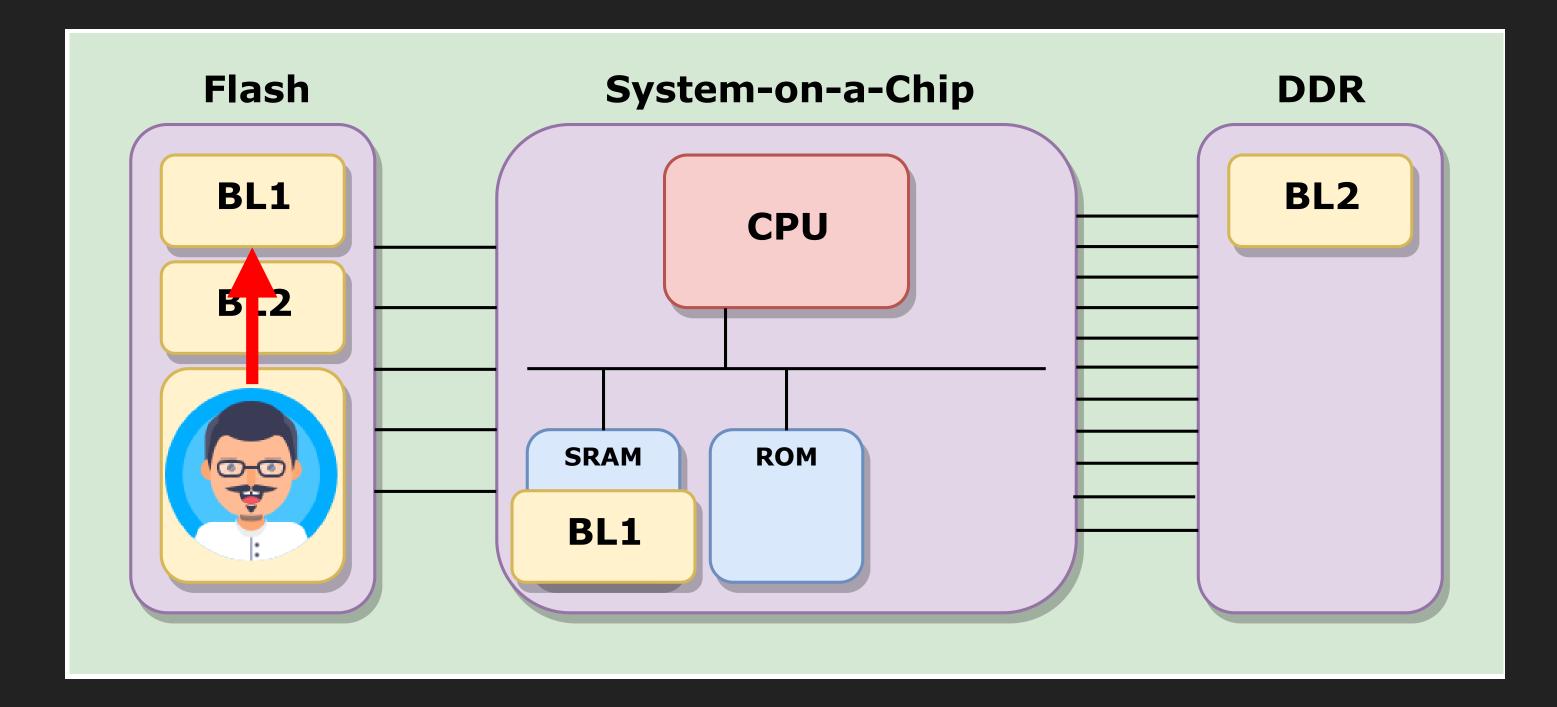


And then, more is loaded and executed...

TWO MAJOR THREATS...

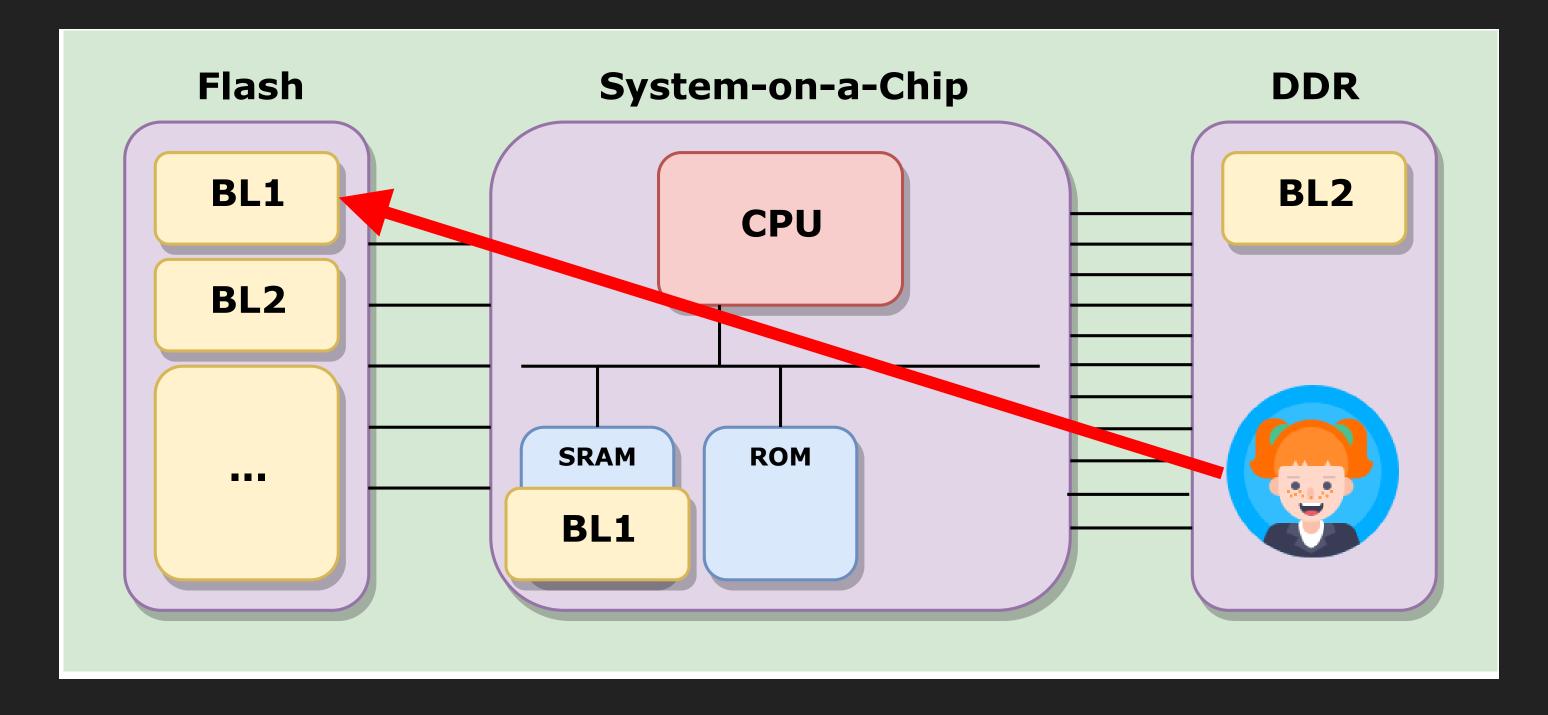


ATTACKERS



Attacker 1: hardware hacker modifies flash

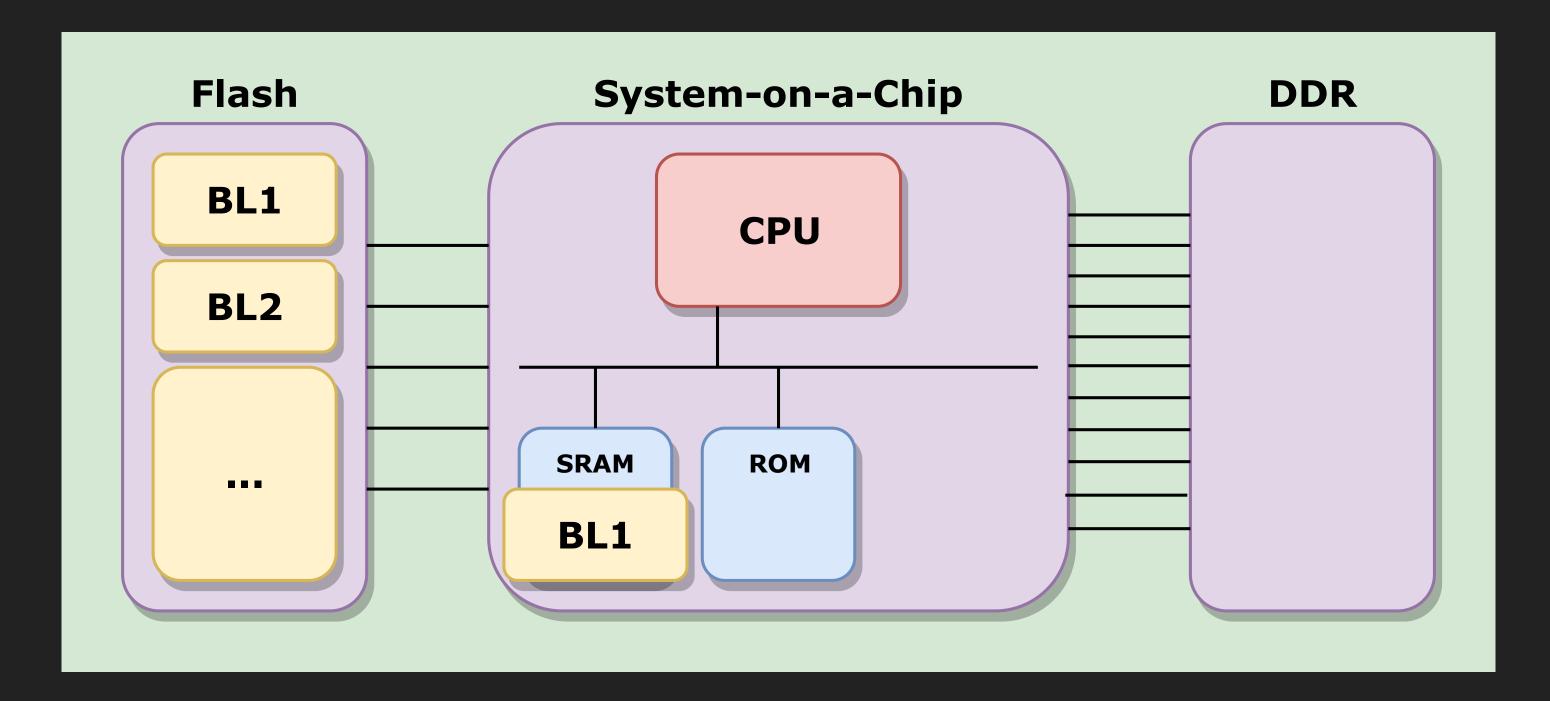
ATTACKERS



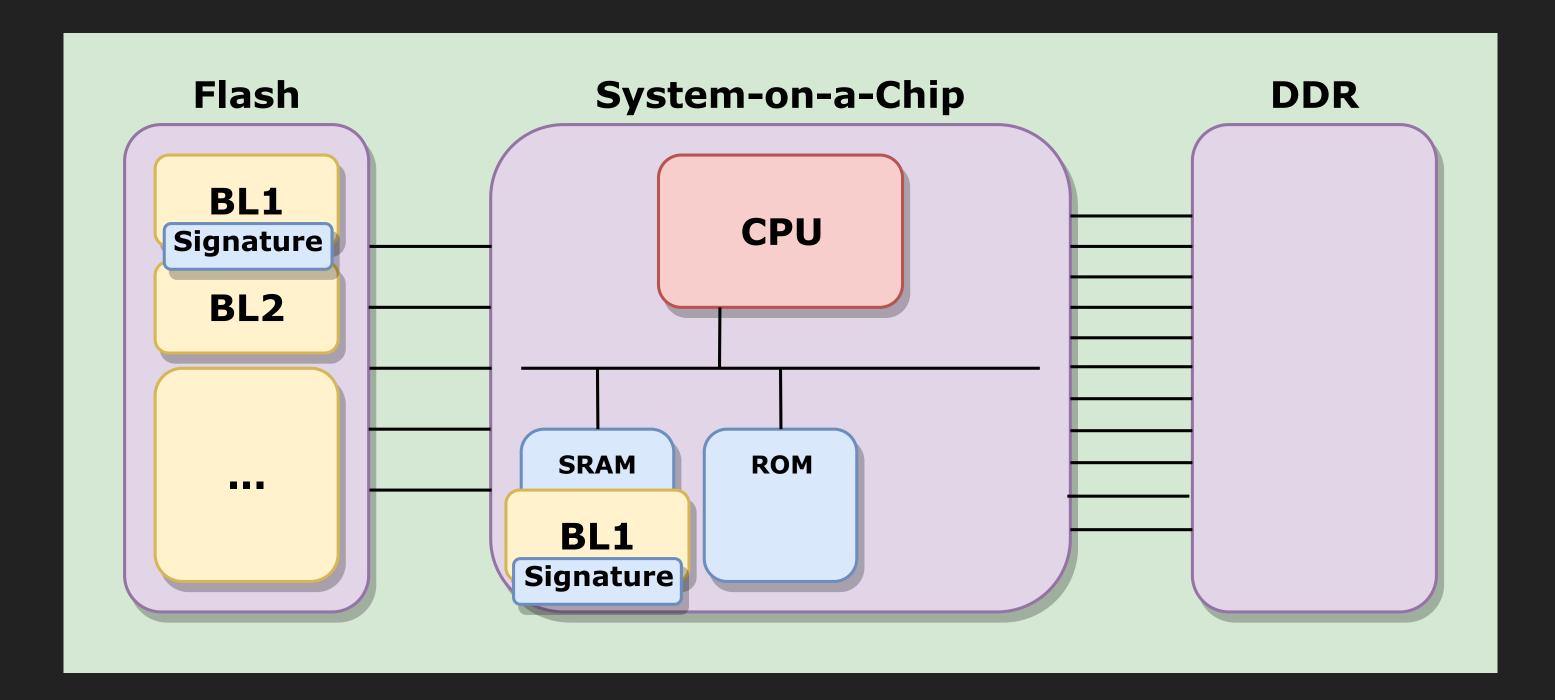
Attacker 2: (remote) software hacker modifies flash

THEREFORE WE NEED SECURE BOOT

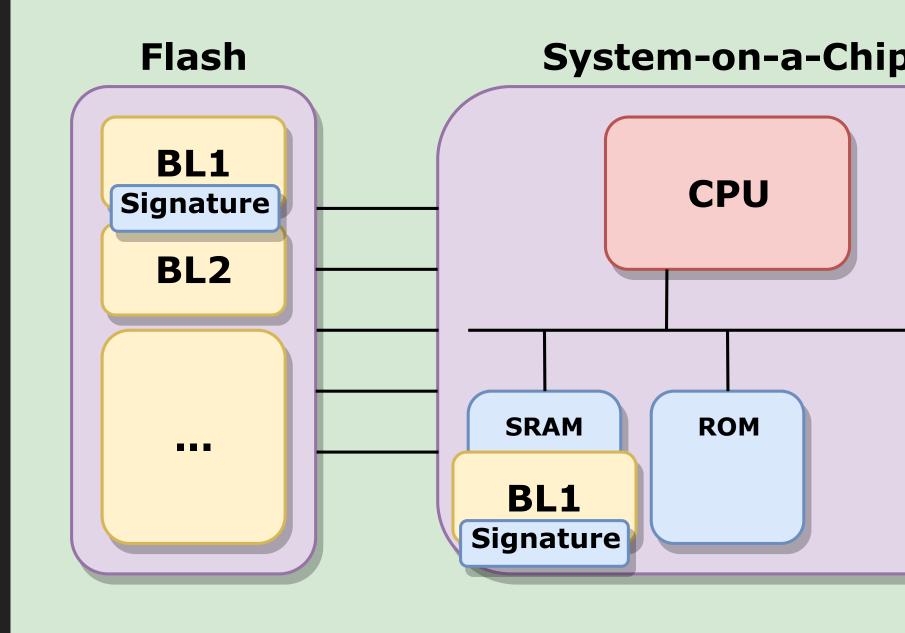
- Authentication of loaded images
- Root of trust embedded in hardware
 - i.e. immutable code and data (e.g. ROM, OTP)



ROM has copied BL1 to SRAM



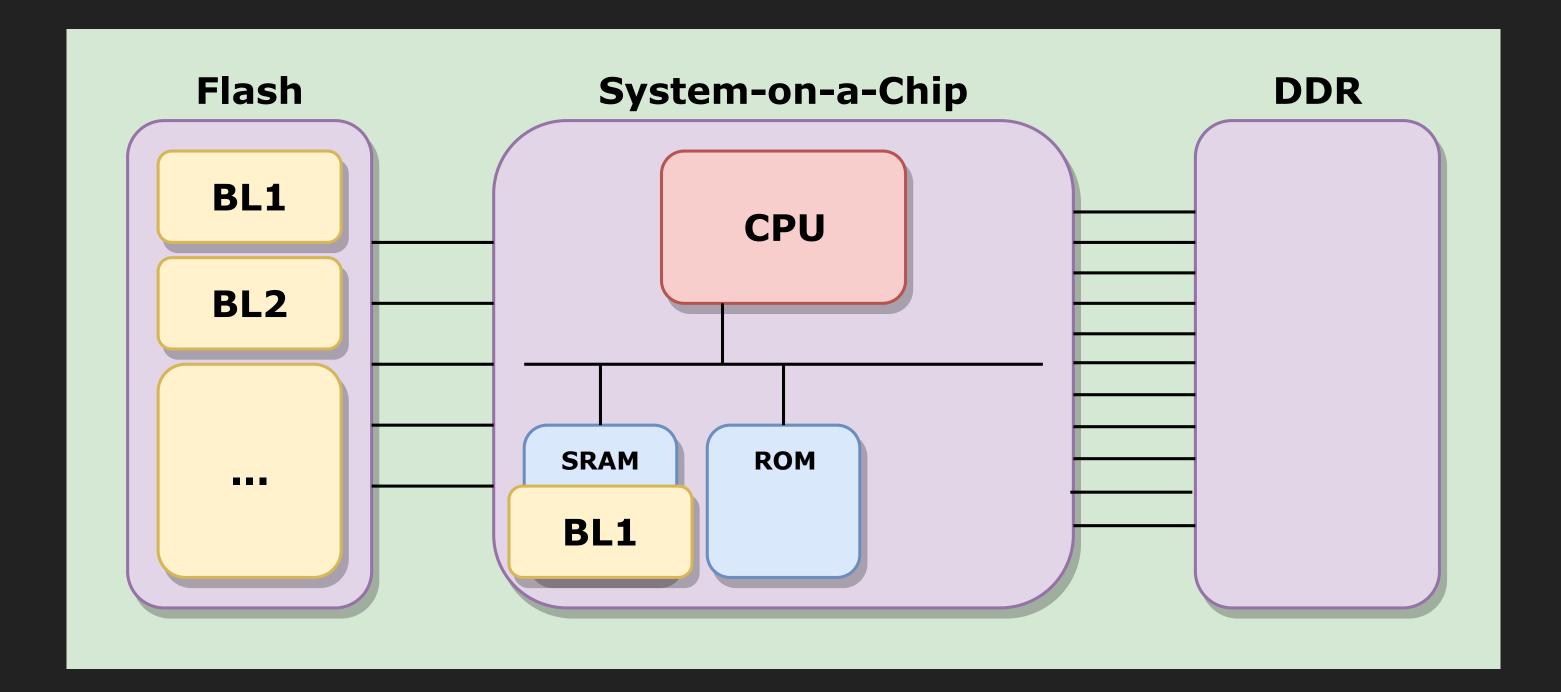
ROM calculates the BL1 hash



ROM compares the hash against the reference from the signature



DDR

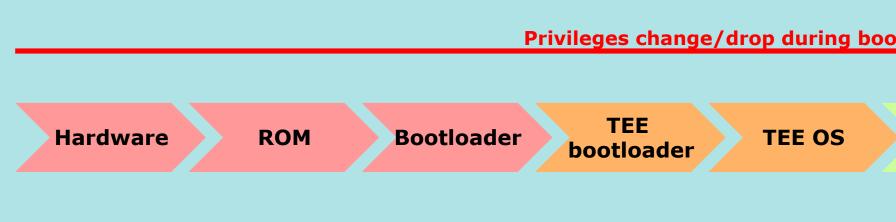


BL1 is executed

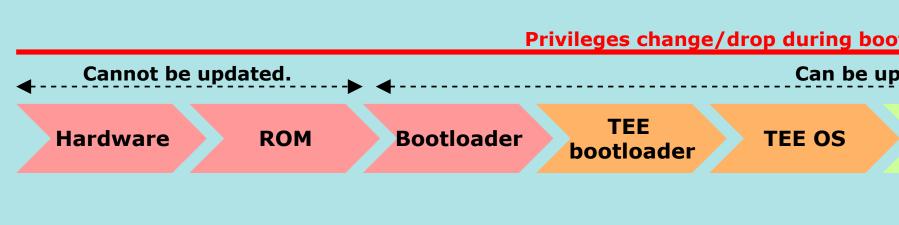


THE REAL WORLD IS A LITTLE MORE COMPLEX...

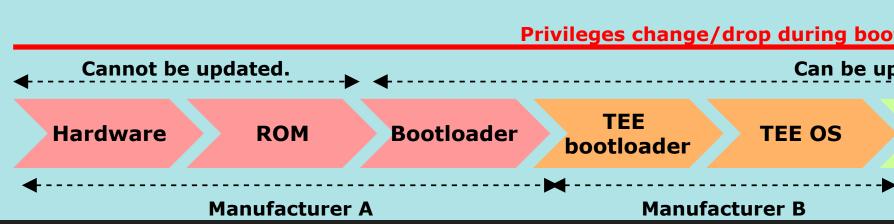




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REE bootloader	REE OS	Apps	



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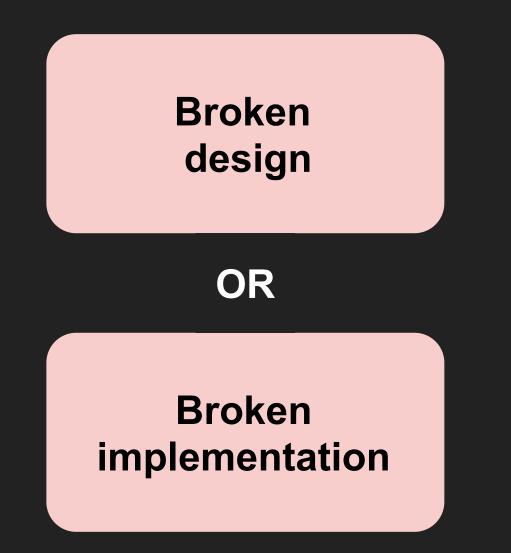
Lots of different interests!

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REE bootloader	REE OS	Apps	
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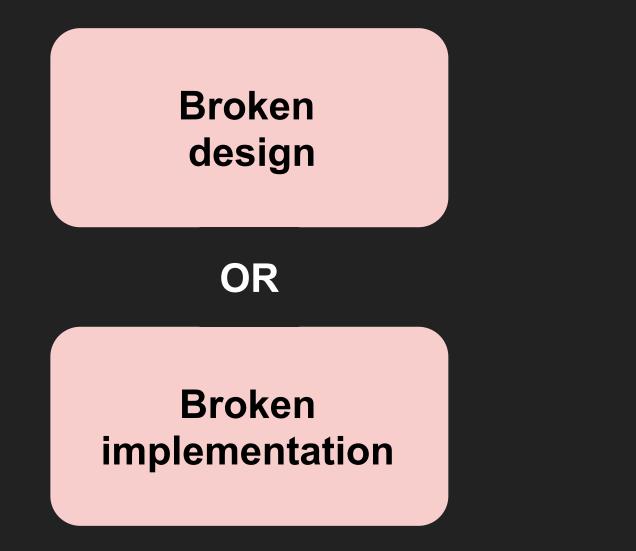
MITIGATING THREATS

- Modifying code/data in flash
- Insecure updates
- Creating a persistent foothold
- Access to keys, code and crypto engines
- Escalating privileges (e.g. REE to TEE)

ATTACK SURFACE



ATTACK SURFACE



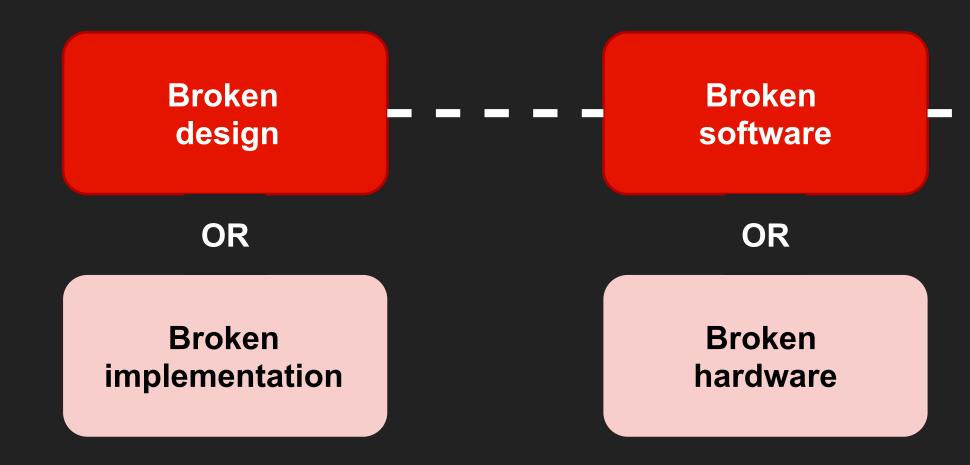
Broken software

OR

Broken hardware

WHAT GOES WRONG IN THE FIELD...

Amlogic S905 SoC BootROM vulnerability



Secure Boot is bypassed, and BootROM is dumped, by downgrading from RSA to SHA

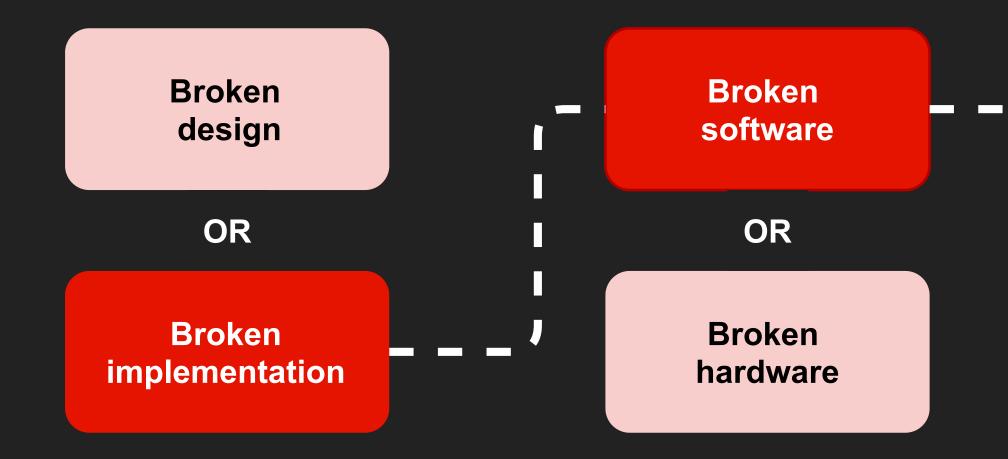
Credit: fredericb

Weak Cryptographic options

MITIGATIONS:

 Do not support weak cryptographic options • Limit the amount of options

Nintendo Switch BootROM vulnerability



Buffer overflow in the USB recovery mode

Credit: fail0verflow and Cease & DeSwitch

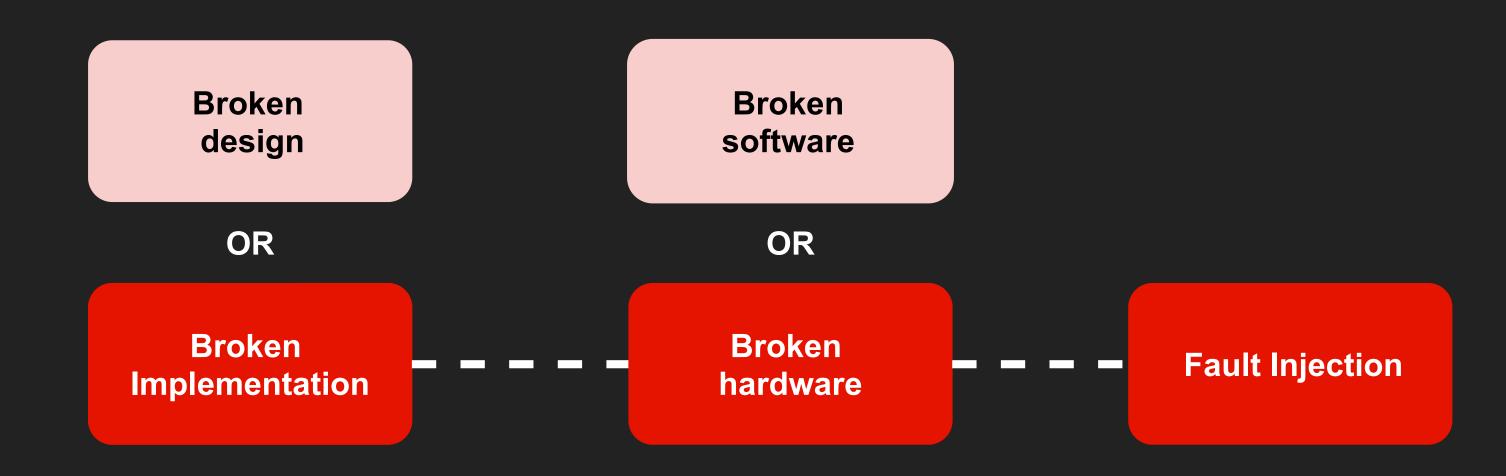
Buffer overflow

MITIGATIONS:

- Write secure software ;)
- Make software exploitation hard
 - i.e. stack cookies, ASLR, CFI, etc.
 - Use memory protections to enforce W^X
 - e.g. MPU, MMU, IOMMU, etc.



SWITCH FAULT INJECTION



SKIP HASH VERIFICATION USING VOLTAGE FAULT INJECTION

FAULT INJECTION (FI)

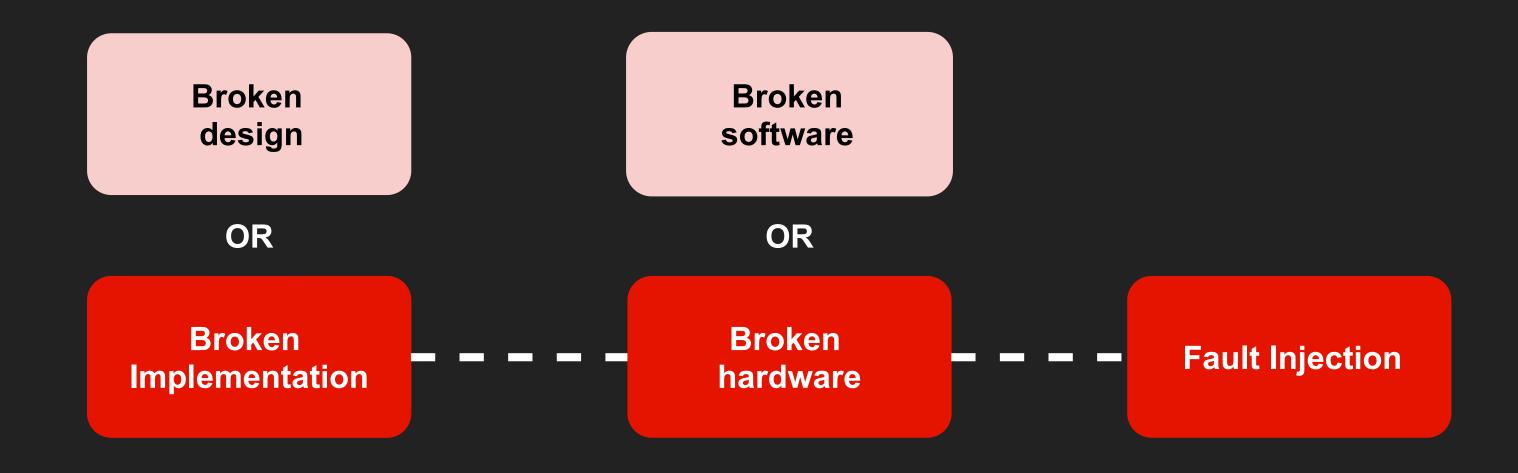
- Make glitches with e.g.: EM, light, clock, power, heat
- Use a glitch to introduce a fault in a device
- Model faults:
 - Instruction skipping
 - Instruction/data corruption

FI ALTERS THE INTENDED BEHAVIOR OF HW AND SW

FAULT INJECTION MITIGATIONS

- Software
 - Redundancy (e.g. double checks)
 - Random delays
- Hardware
 - Redundancy
 - Glitch detectors
 - Clock randomization

Viva La Vita Vida fault injection attack



Introducing a classic buffer overflow using Voltage Fault Injection

Credit: Yifan Lu and Davee @ 35c3

MITIGATIONS:

It's Fault injection so use FI mitigations It's Software exploit so use exploit mitigations

DESIGNING SECURE BOOT AINT EASY!

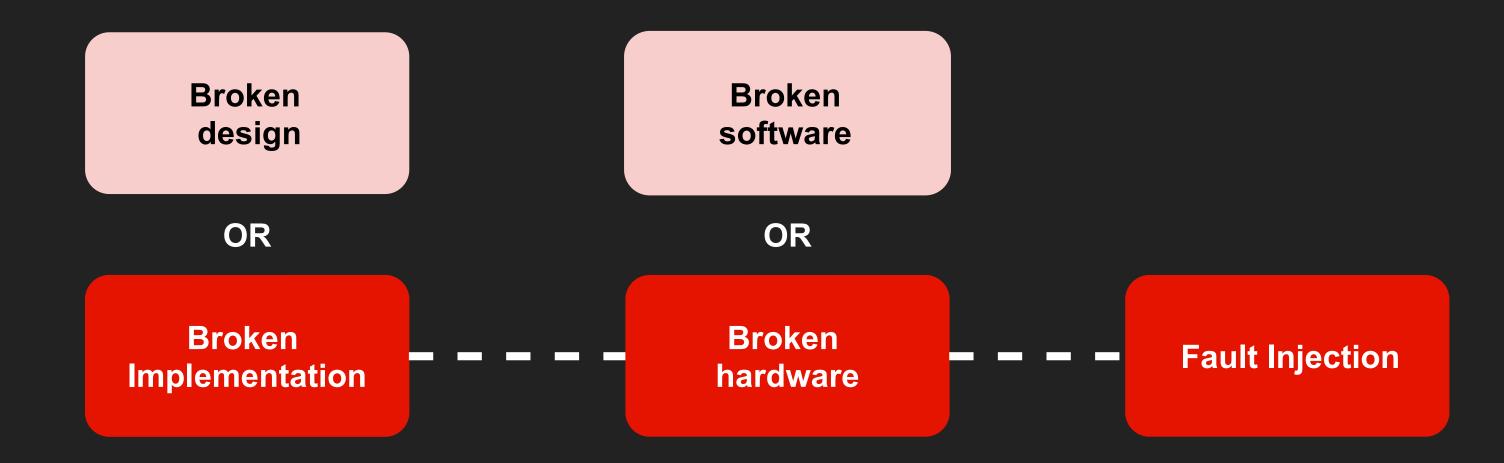
ESPECIALLY CONSIDERING THE CONSTRAINTS... Initializing hardware Interfacing with peripherals Performance Code size Keeping engineering cost low Recoverability Customer needs

IT'S IMPORTANT TO GET IT RIGHT

WRONG SECURITY IS EXPENSIVE Tape out Crisis management PR damage Time to market Recall of devices/unsold inventory Additional engineering time

HAS THE WORLD SEEN IT ALL?

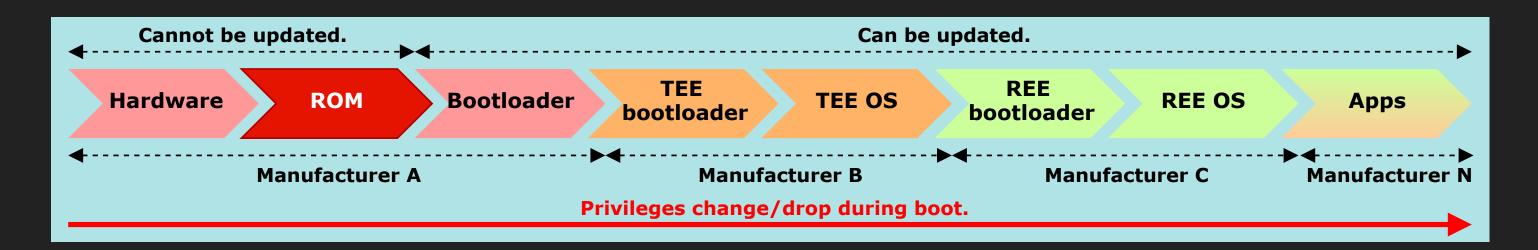
FAULT INJECTION ON OTP TRANSFER



Attacking Secure Boot before any code is executed!

LET'S LOOK AT THIS ONE IN DETAIL

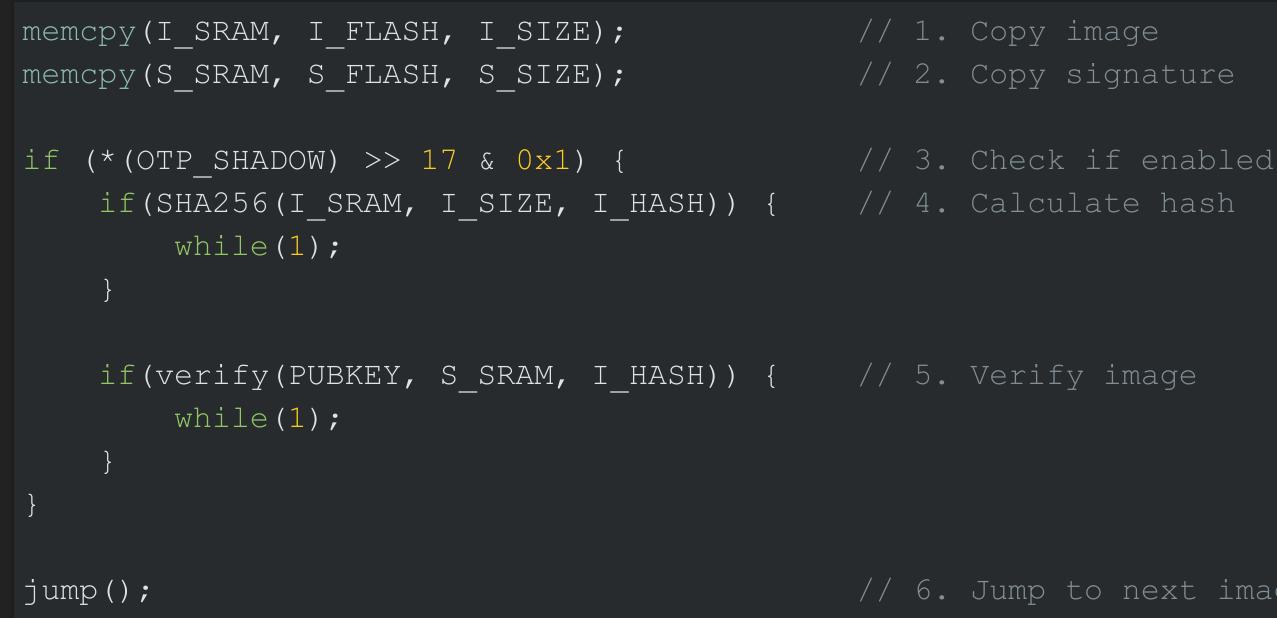
OTP AND SECURE BOOT



ROM code uses values from OTP for enabling/disabling security features.



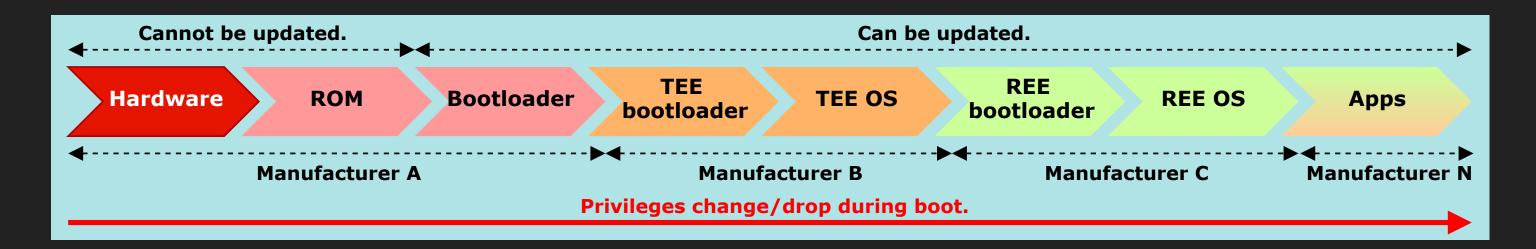
EXAMPLE



Value stored in shadow registers. Populated by OTP Transfer.

// 6. Jump to next image

POPULATING SHADOW REGISTERS

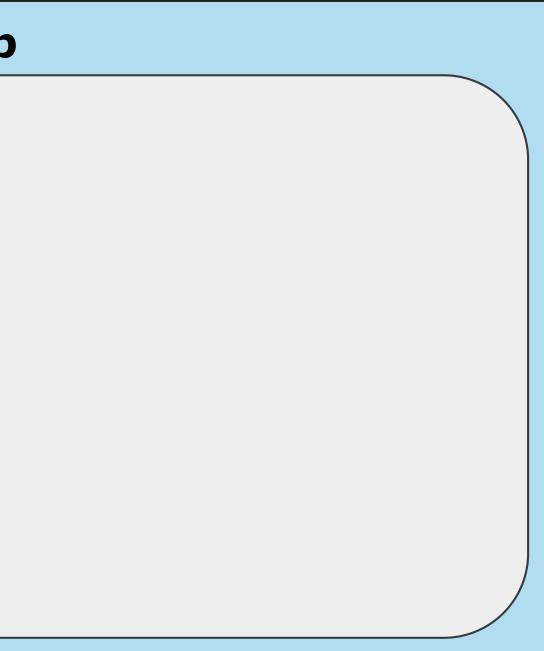


OTP Transfer performed in hardware. BEFORE any ROM code is executed.

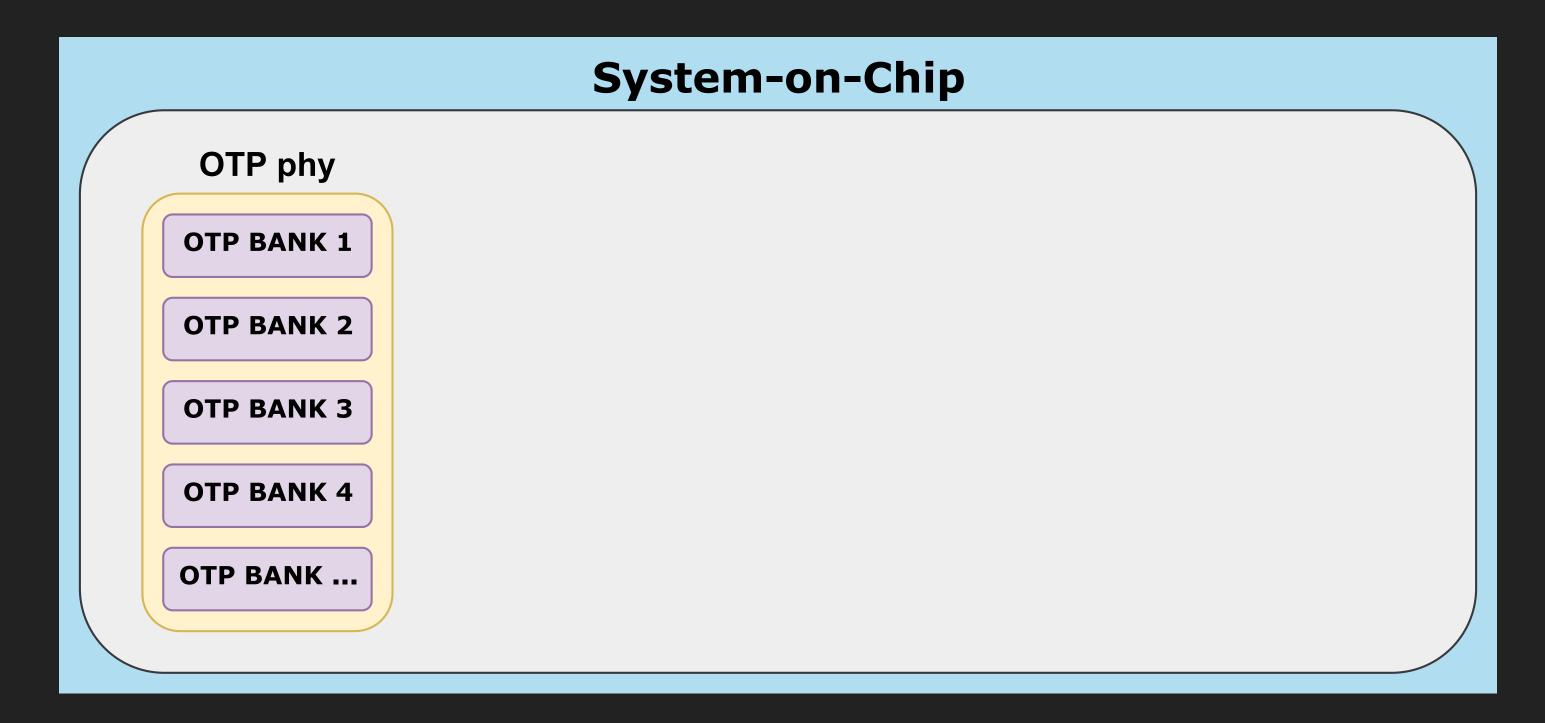
OTP TRANSFER 1/5

System-on-Chip

A typical System-on-Chip (SoC)

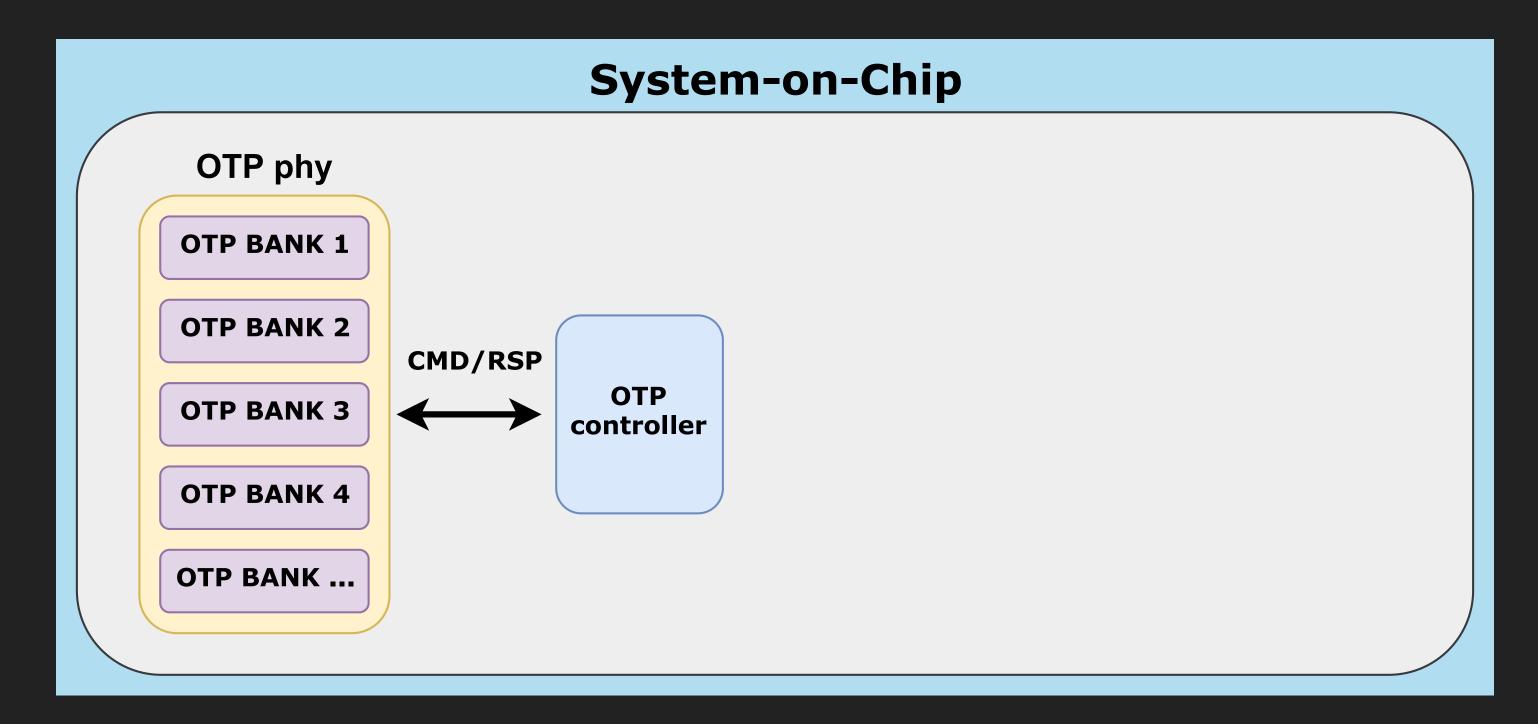


OTP TRANSFER 2/5



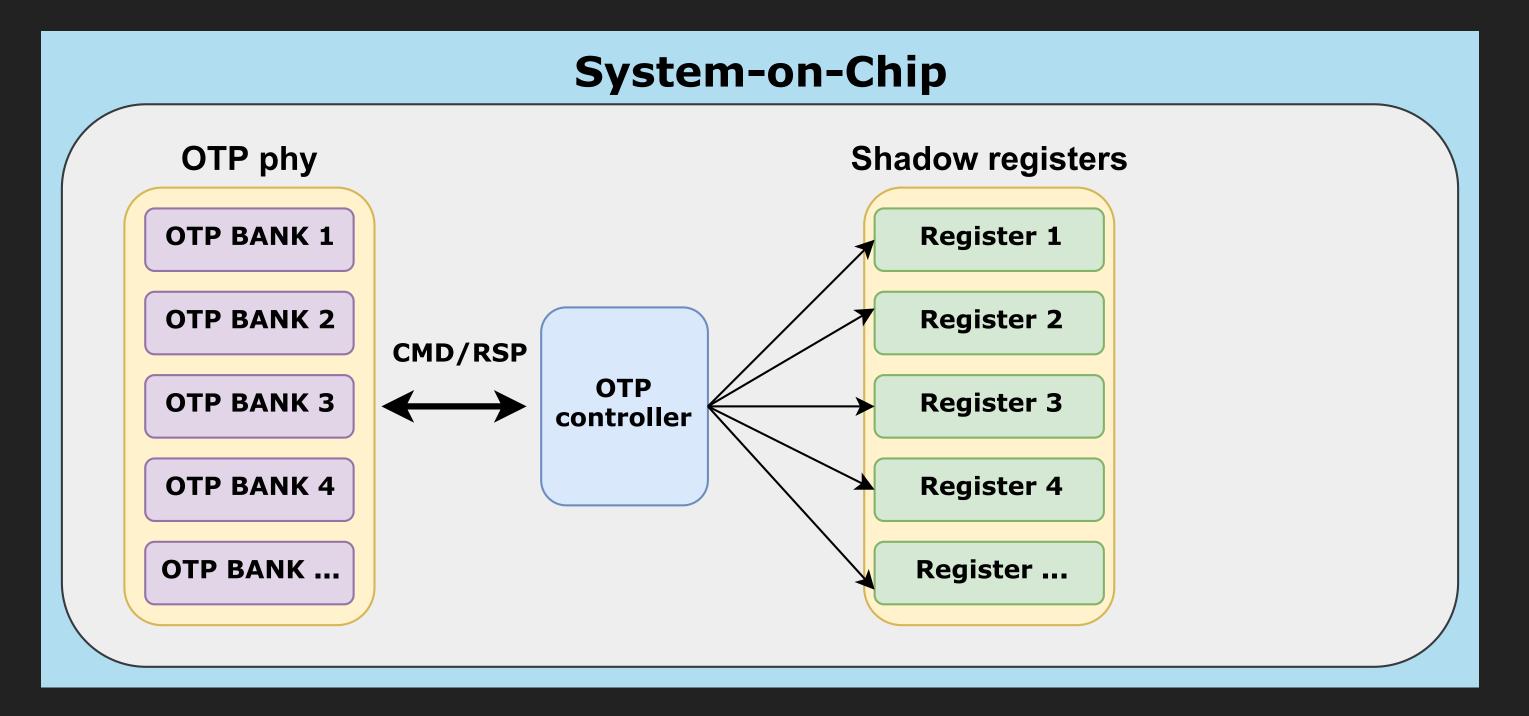
Contains a special OTP hardware block

OTP TRANSFER 3/5



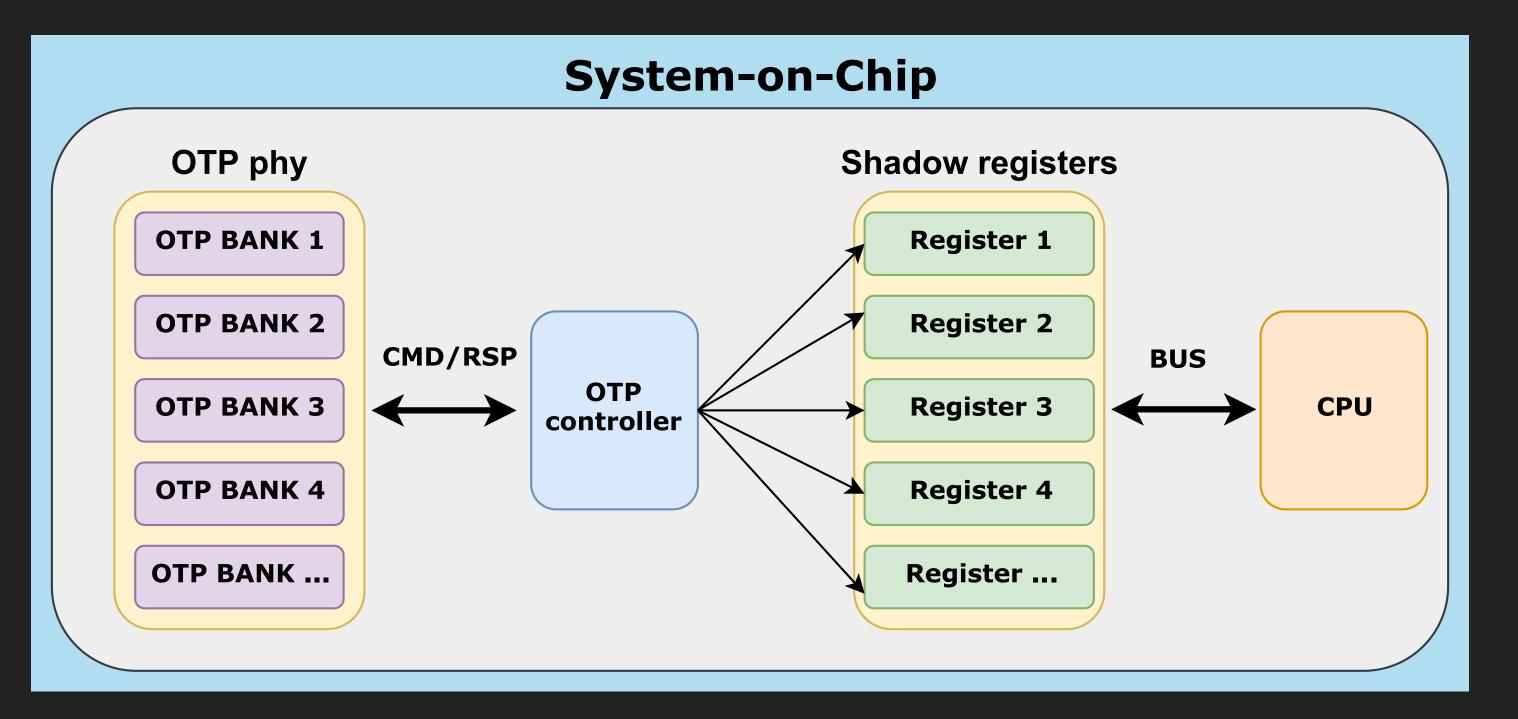
Which is wrapped by a hardware controller

OTP TRANSFER 4/5



This controller copies the OTP values to dedicated registers after SoC reset

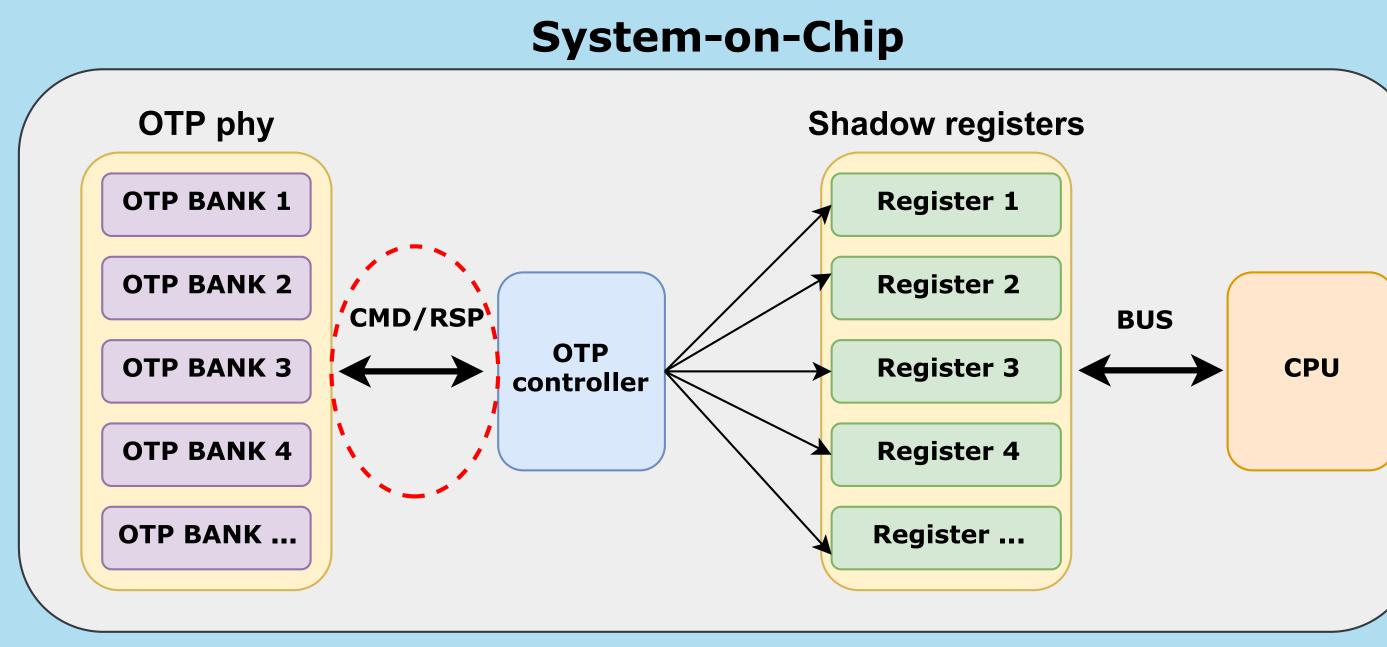
OTP TRANSFER 5/5



CPU is released from reset. Shadow registers can be read using system bus.

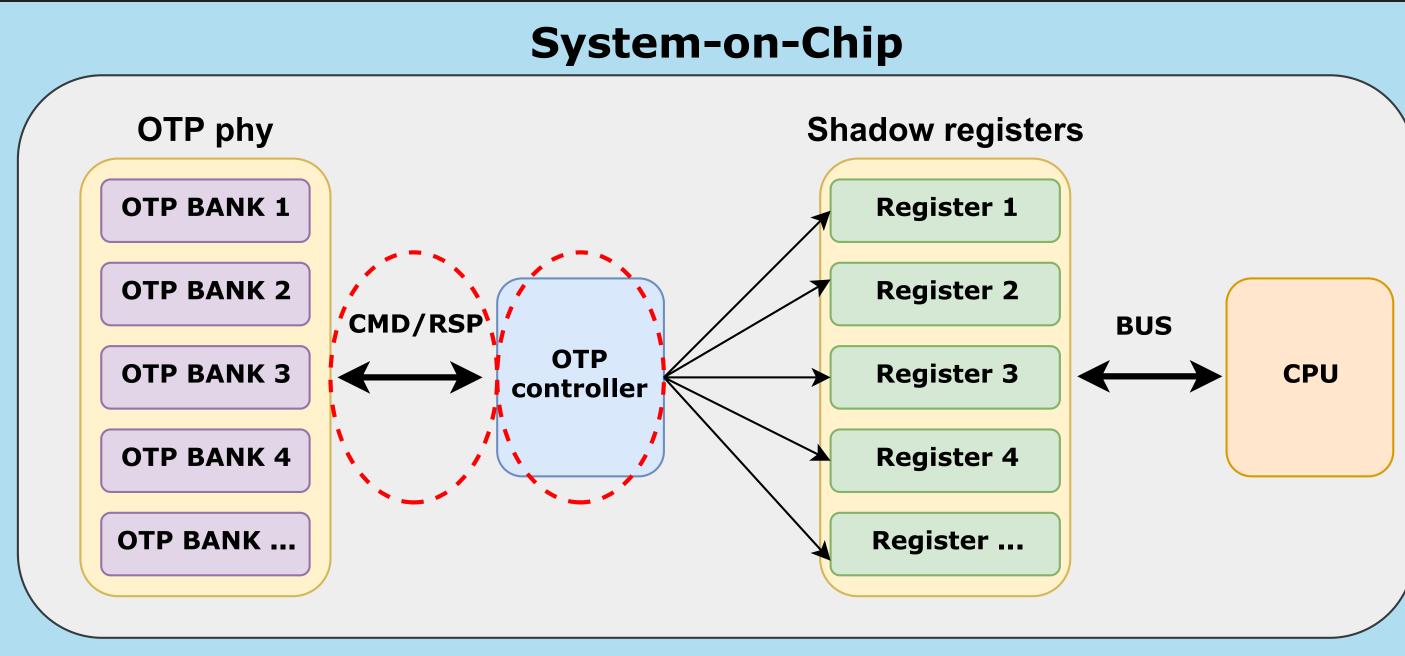
WHERE CAN WE ATTACK?

ANYWHERE!



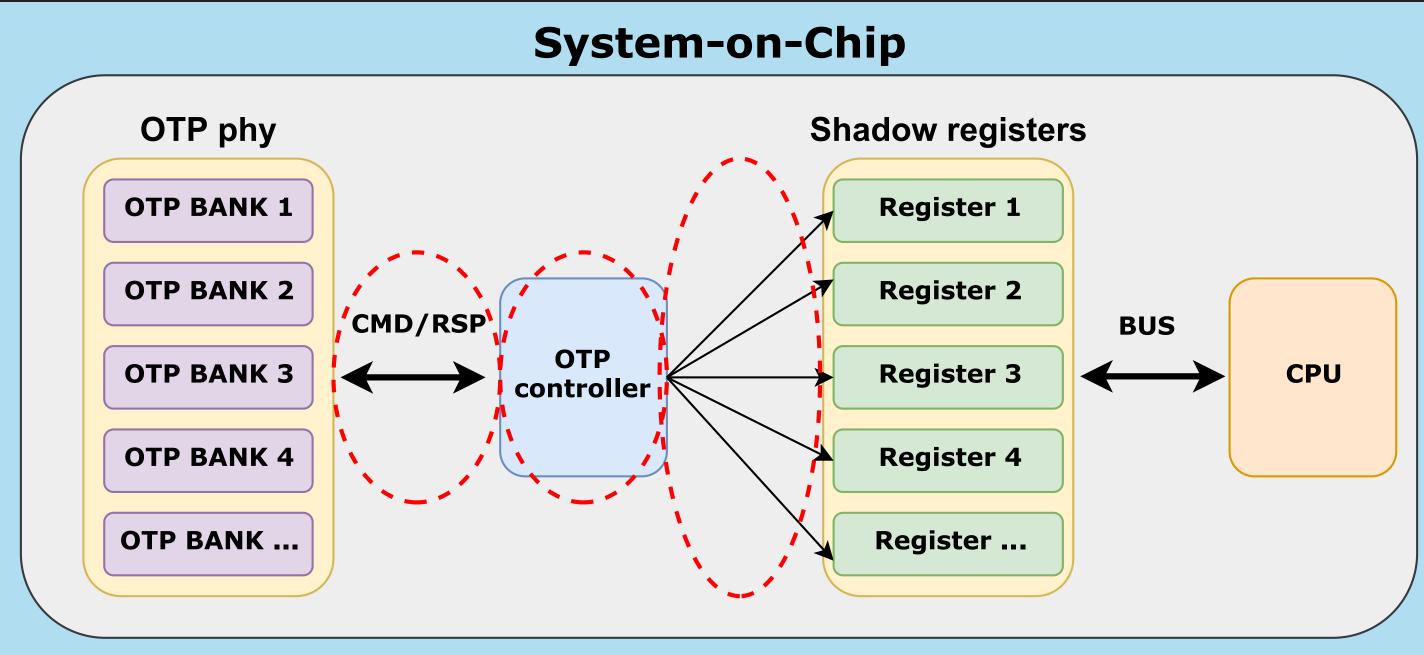
Attack the bus between the OTP PHY and the OTP controller.

ANYWHERE!



Attack the OTP controller directly.

ANYWHERE!

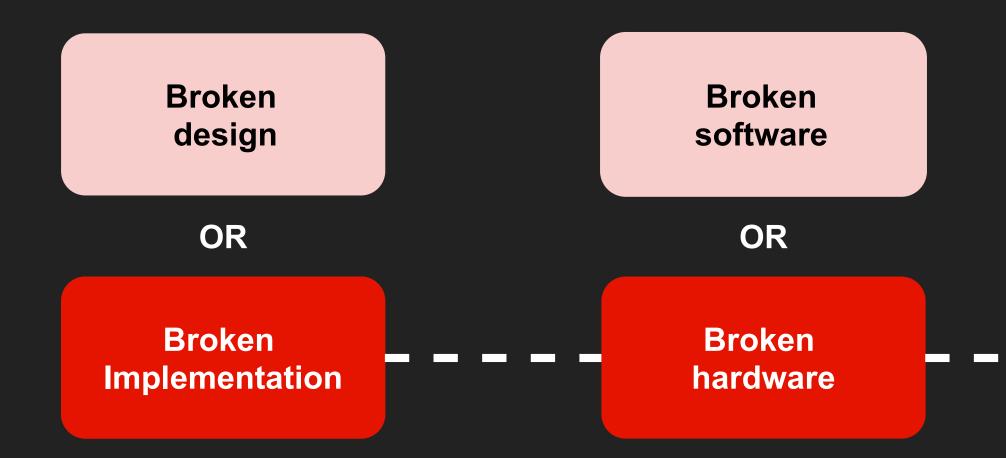


Attack the bus between the OTP controller and the shadow registers.

WE CAN AFFECT SIGNATURE VERIFICATION AND/OR **STAGE ENCRYPTION** BYPASSING (ENCRYPTED) SECURE BOOT

THAT WAS FUN; LET'S DO ANOTHER ONE!

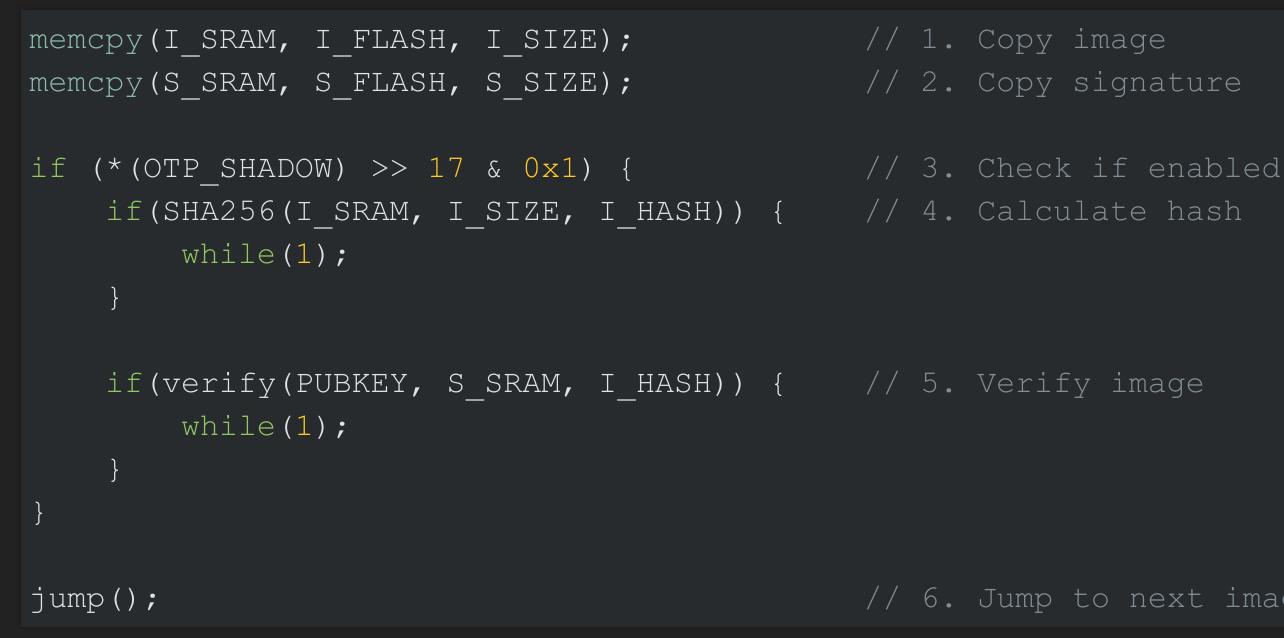
FAULT INJECTION ON ENCRYPTED SECURE BOOT



...WITHOUT AN ENCRYPTION KEY!

Fault Injection

SIGNATURE VERIFICATION



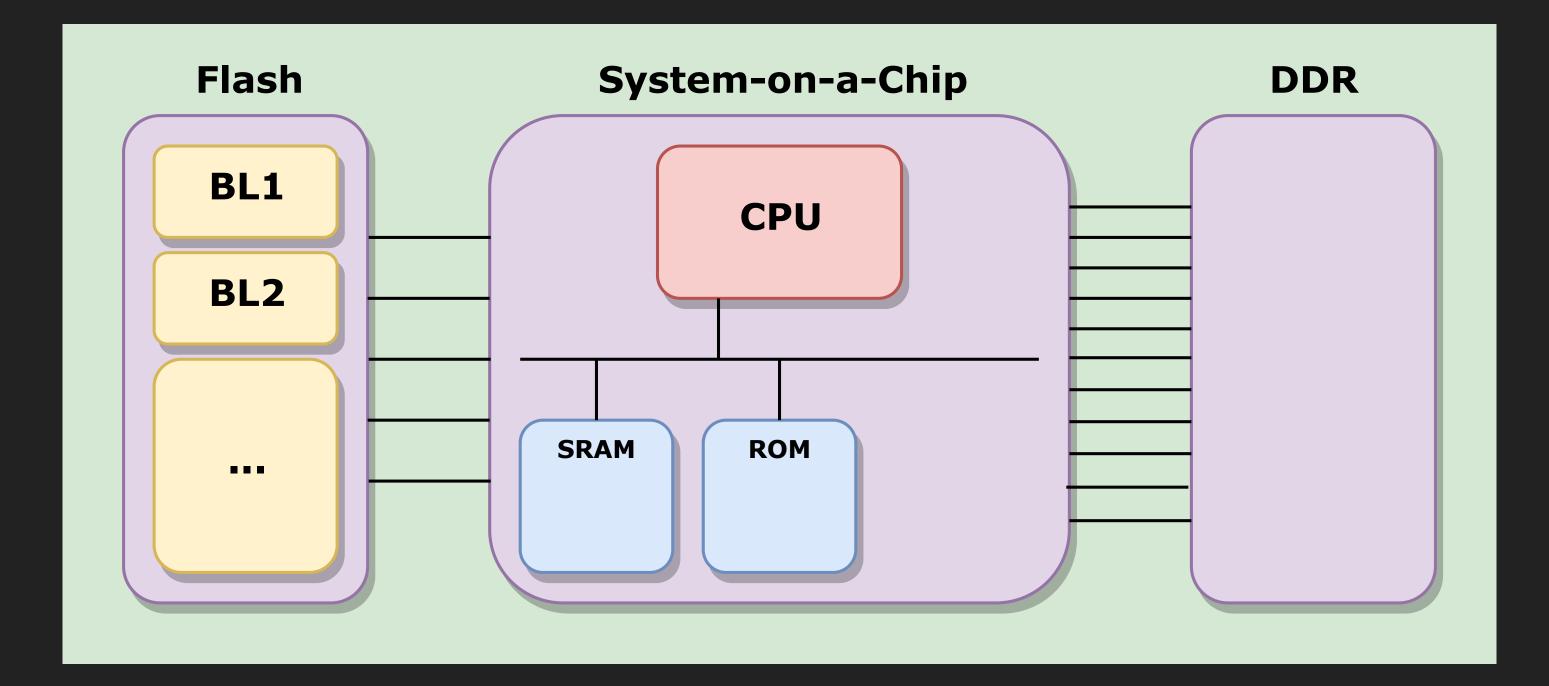
// 6. Jump to next image

FAULT INJECTION FAULT MODEL "Instruction skipping"

- Faults can cause "instruction not to be executed"
- Inaccurate but sufficient
- Widely adopted (by academia and industry)
- Useful for affecting the code flow

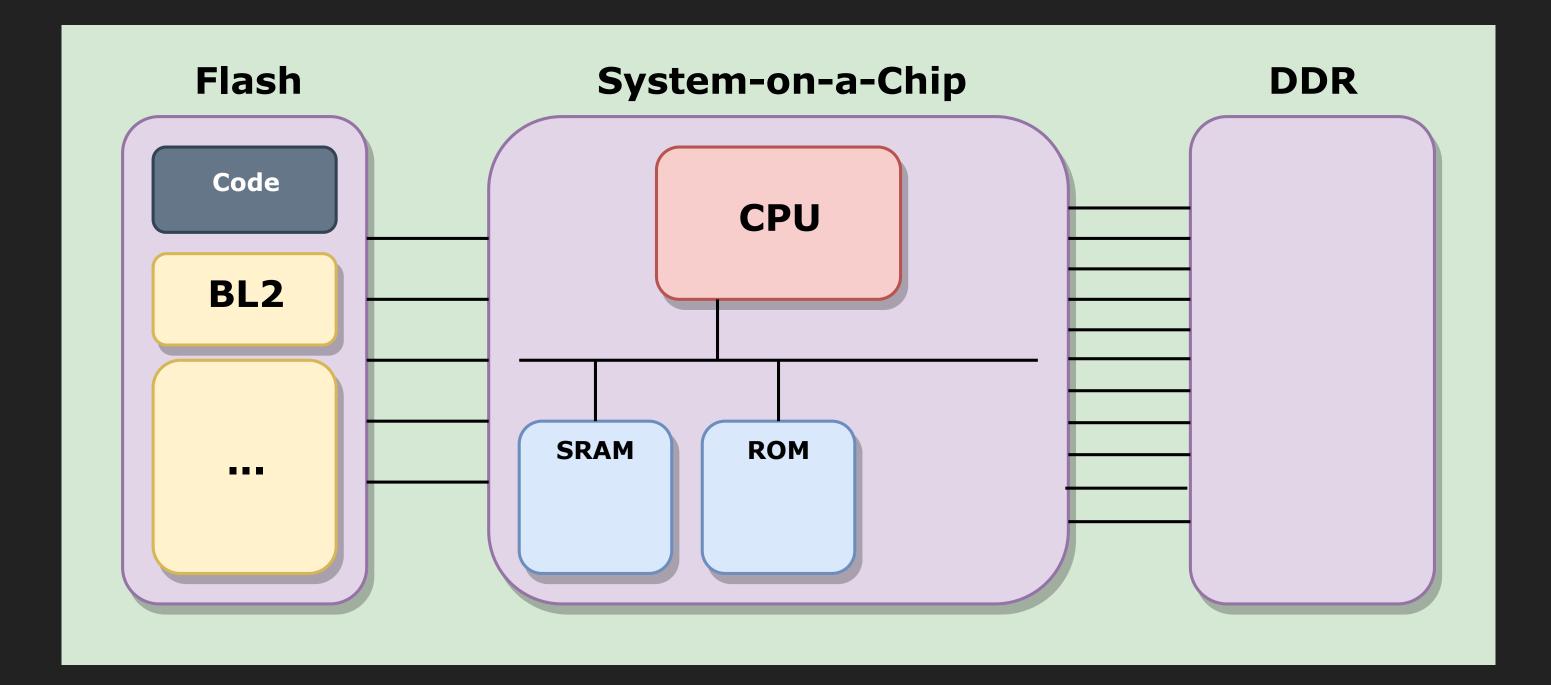
LET'S USE IT FOR BYPASSING SECURE BOOT!

A TEXTBOOK ATTACK 1/3



Device is turned off

A TEXTBOOK ATTACK 2/3



Replace BL1 with a malicious image

A TEXTBOOK ATTACK 3/3

```
memcpy(I_SRAM, I_FLASH, I_SIZE); // 1. Copy image
memcpy(S SRAM, S FLASH, S SIZE); // 2. Copy signature
if (* (OTP_SHADOW) >> 17 & 0x1) { // 3. Check if enabled
   if(SHA256(I_SRAM, I_SIZE, I_HASH)) { // 4. Calculate hash
       while(1);
   if (verify (PUBKEY, S SRAM, I HASH)) { // 5. Glitch here!
       while(1);
jump();
```

Skip verify function call and boot an malicious image

// 6. Jump to next image

GLITCH AT THE RIGHT MOMENT AND PROFIT!

WHAT IF BL1 IS ENCRYPTED?

ENCRYPTED SECURE BOOT

```
memcpy(I_SRAM, I_FLASH, I_SIZE); // 1. Copy image
decrypt(SYM_KEY, I_SRAM, I_SIZE); // NEW: Decrypt image
memcpy(S SRAM, S FLASH, S SIZE); // 2. Copy signature
if (*(OTP SHADOW) >> 17 & 0x1) { // 3. Check if enabled
   if (SHA256 (I SRAM, I SIZE, I HASH)) { // 4. Calculate hash
       while(1);
   if (verify (PUBKEY, S SRAM, I HASH)) { // 5. Glitch here!
       while(1);
jump();
```

The image is decrypted after it is copied and before it is verified!

// 6. Jump to next image

THE MISSING KEY...

Encryption key needed for creating a malicious image

THAT'S WHY...

FI attacks are often considered infeasible when encrypted Secure Boot is used.

UNTIL NOW!

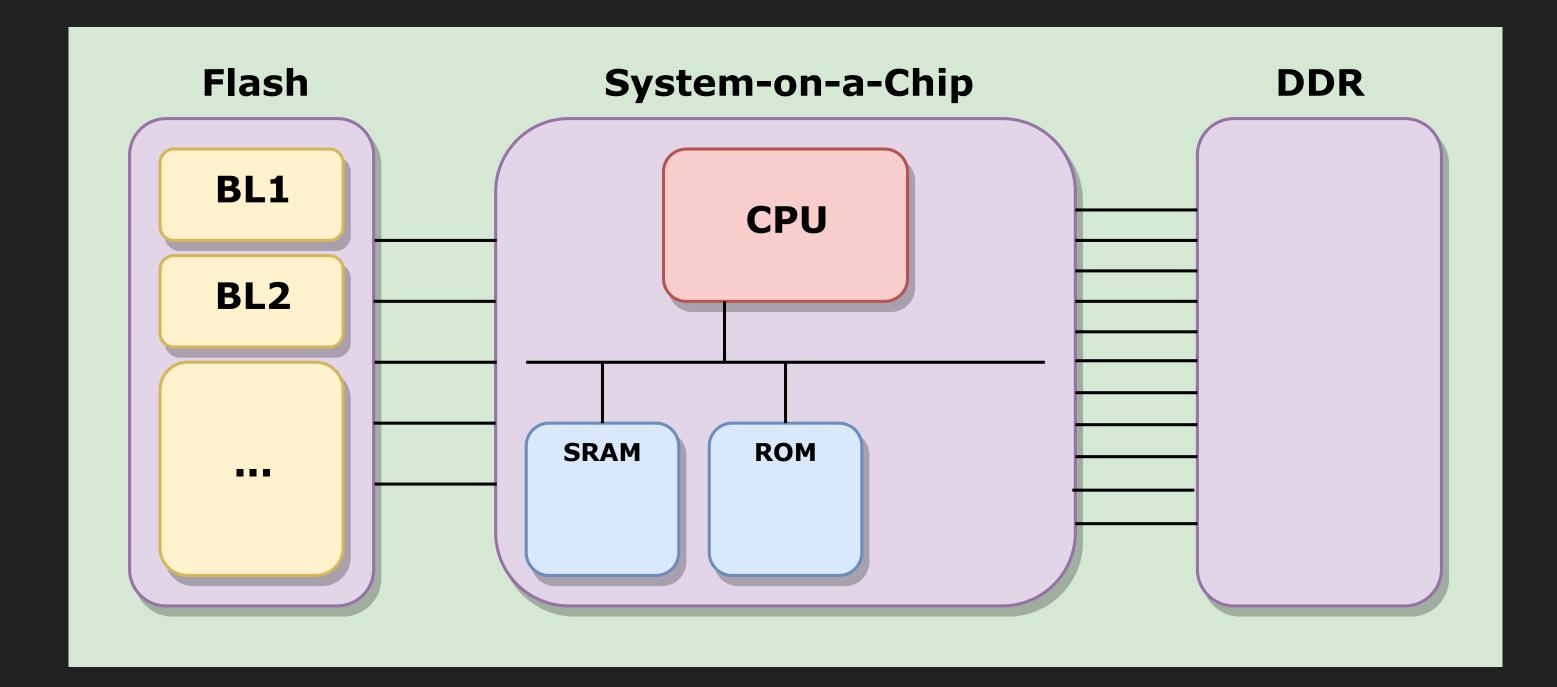


FAULT INJECTION FAULT MODEL

"Instruction corruption"

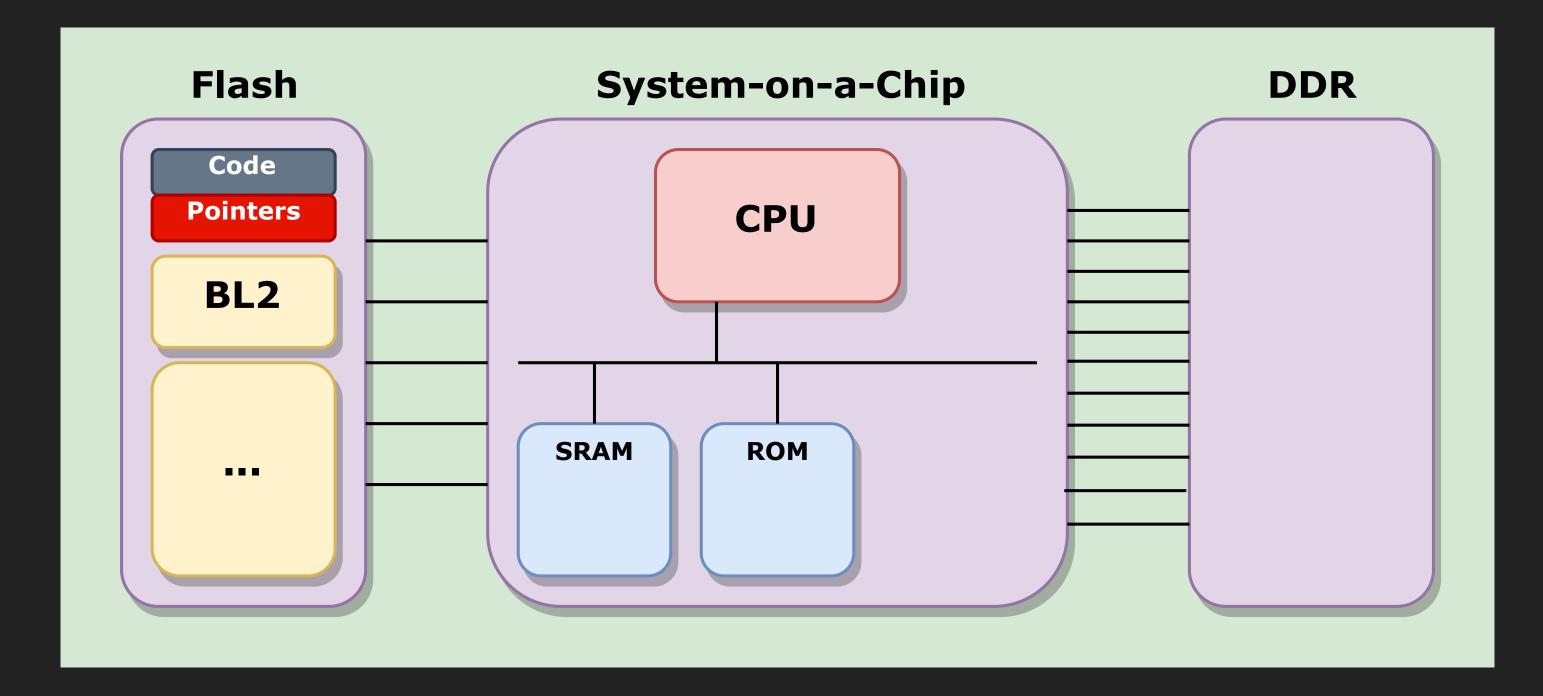
- Faults can modify instructions
- Destination register could be changed
- Fairly new application
- Great for modifying code and getting control

BYPASSING ENCRYPTED SECURE BOOT 1/4



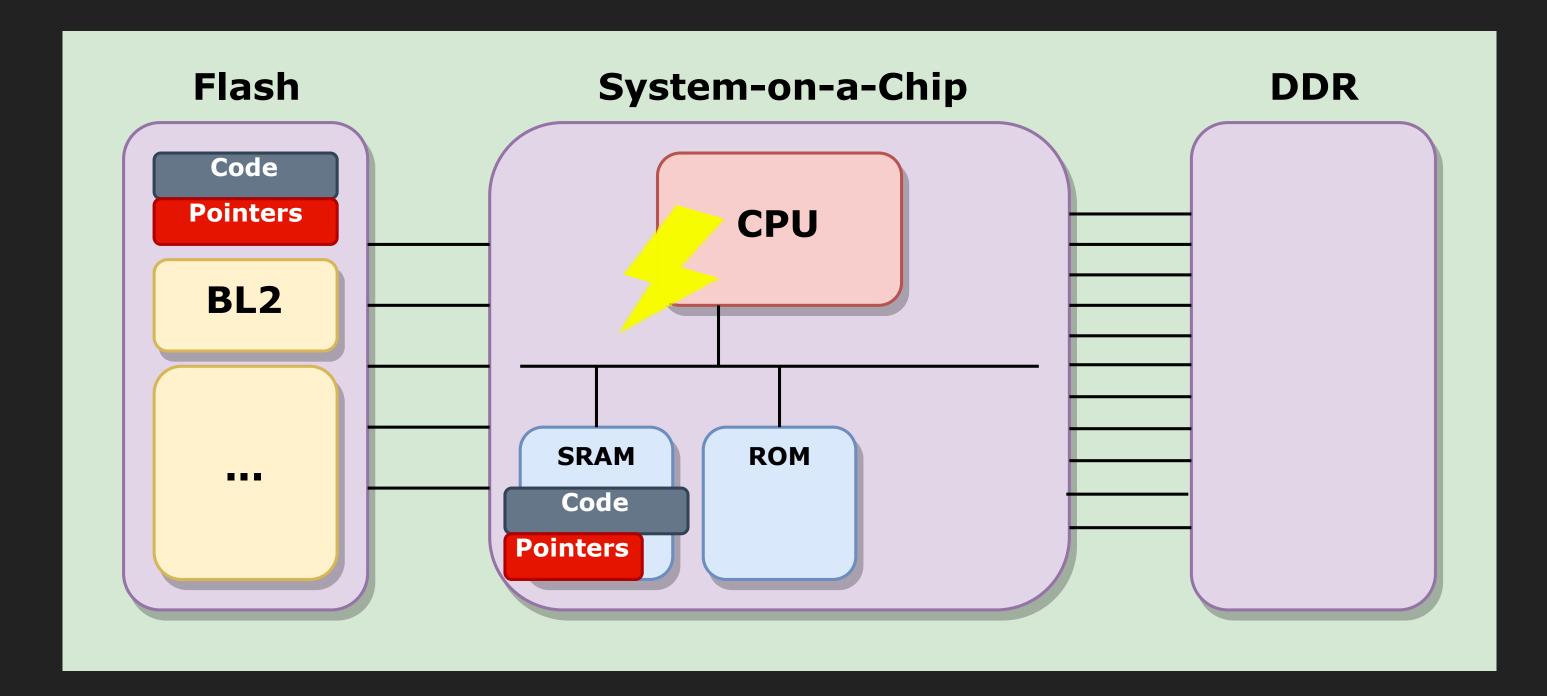
Device is turned off.

BYPASSING ENCRYPTED SECURE BOOT 2/4



Replace encrypted BL1 with plain text code and pointers to SRAM.

BYPASSING ENCRYPTED SECURE BOOT 3/4



Glitch is injected after code copy and while pointers are being copied.

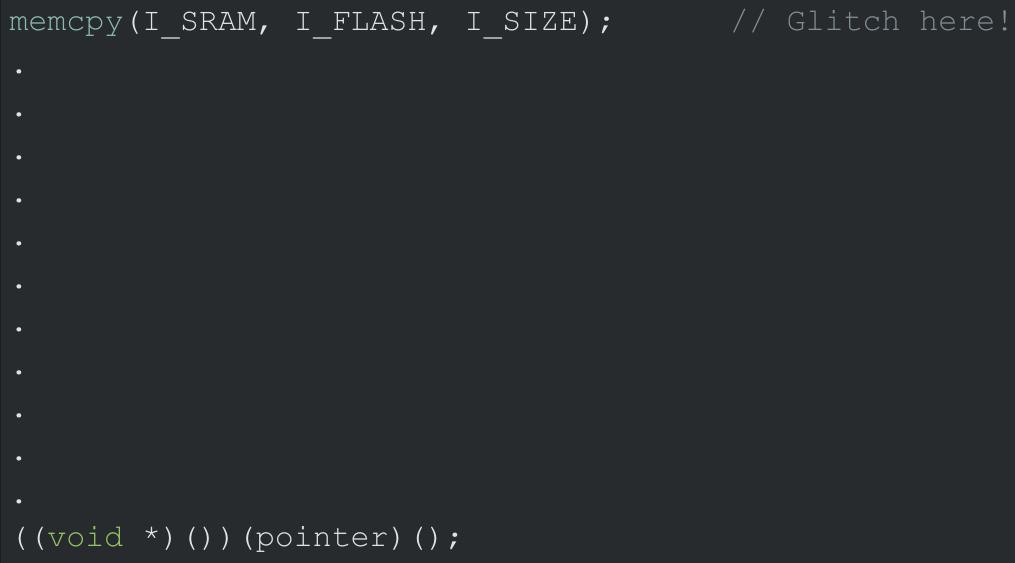
BYPASSING ENCRYPTED SECURE BOOT 4/4

```
memcpy(I_SRAM, I_FLASH, I_SIZE); // Glitch here!
decrypt(SYM KEY, I SRAM, I SIZE); // Before decryption
memcpy(S SRAM, S FLASH, S SIZE); // and
if(SHA256(I_SRAM, I_SIZE, I_HASH)) { // before
   while(1);
if(verify(PUB KEY, S SRAM, I HASH)) { // verification!
   while(1);
jump();
```

Glitch during pointers copy to assign a pointer to the program counter (PC).

// CPU will never reach here

RESULTING CODE EXECUTION



Control flow is hijacked. The decryption and verification of the image is bypassed!

CONCRETELY SAID...

WE TURN ENCRYPTED SECURE BOOT INTO PLAINTEXT UNPROTECTED BOOT USING A SINGLE GLITCH AND NO KEY!

PWN3D!

• Timing no so relevant

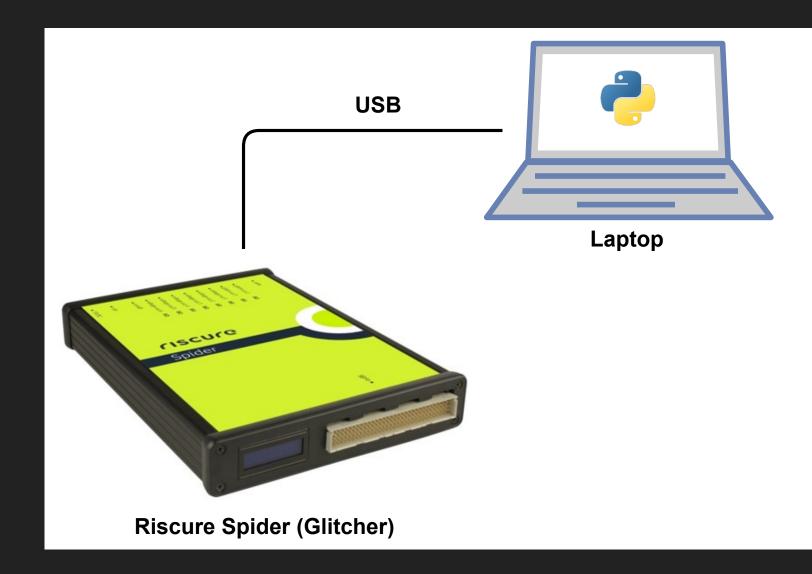
- Full PC control
- Bypass any SW FI countermeasure

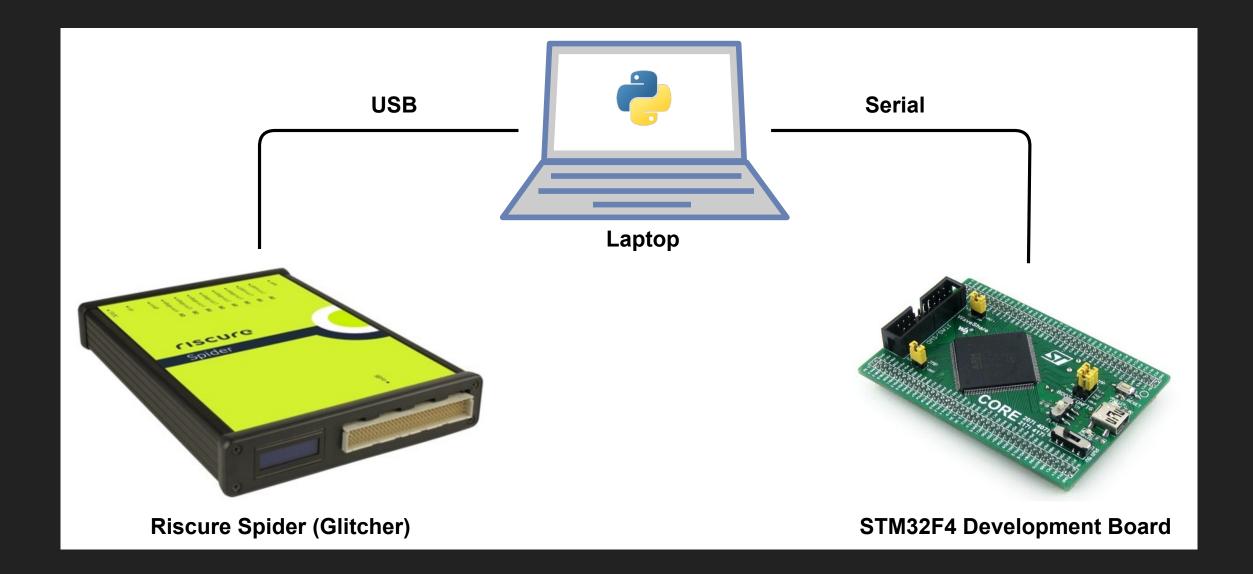
FAULT INJECTION DEMO ON ENCRYPTED SECURE BOOT!

Important: We are attacking a demo implementation!

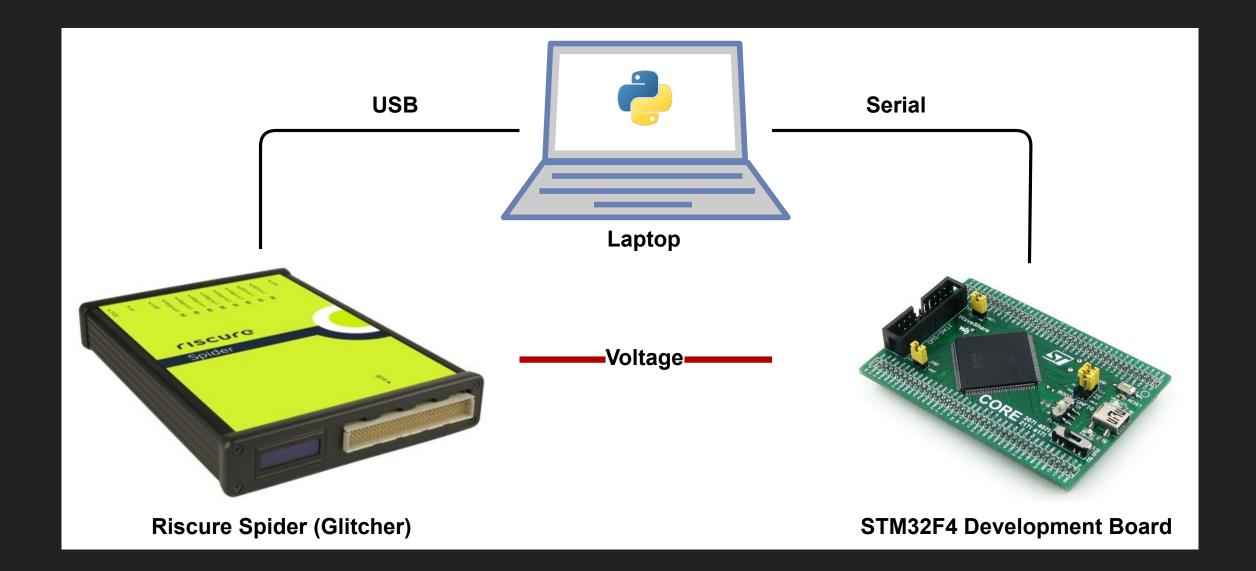


Riscure Spider (Glitcher)

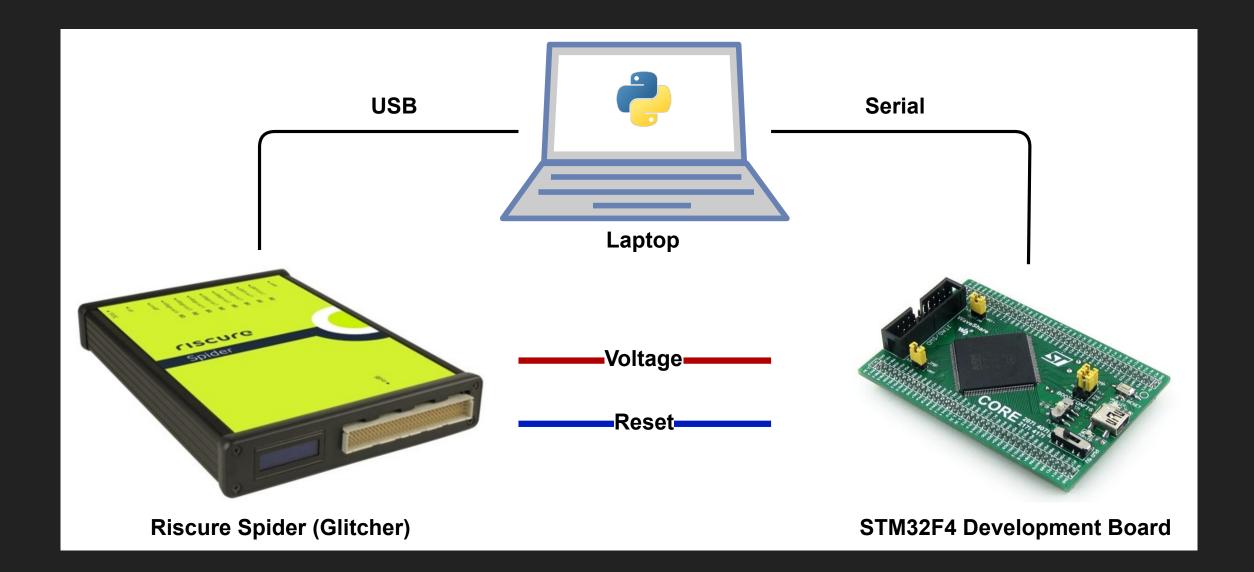












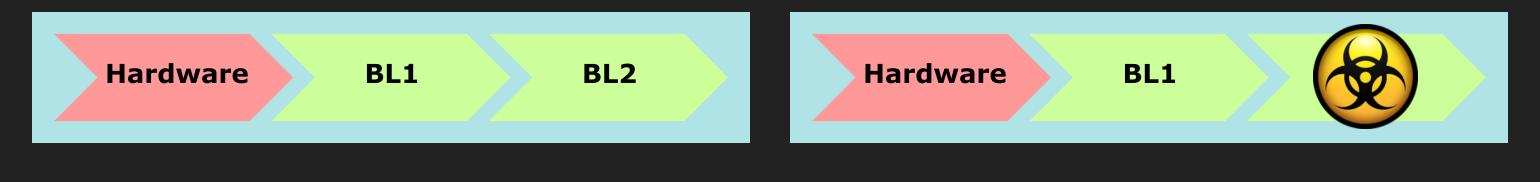


REAL WORLD FI SETUP



Even for simple setups there are cables everywhere...

FLASH IMAGEMODIFICATIONVALID IMAGEMALICIOUS IMAGE

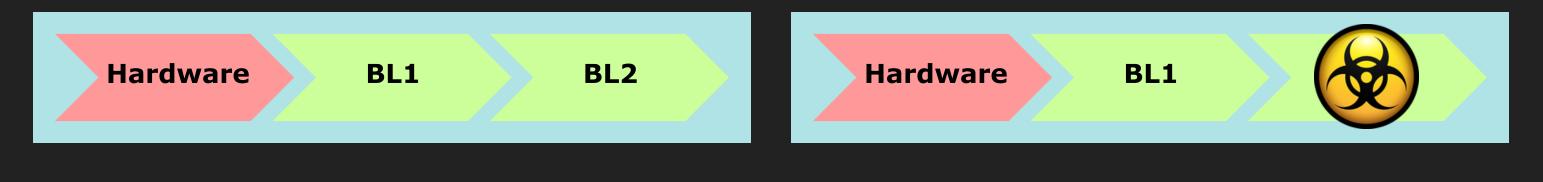


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BL1 loads, decrypts and authenticates BL2 successfully

BL1 loads, decrypts but fails to authenticate BL2

FLASH IMAGEMODIFICATIONVALID IMAGEMALICIOUS IMAGE



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BL1 loads, decrypts and authenticates BL2 successfully

BL1 loads, decrypts but fails to authenticate BL2

TARGET BEHAVIOR

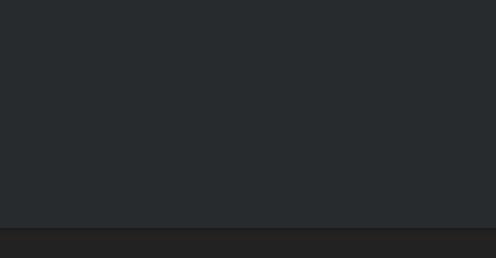
Valid image

- [BL1]: Successfully started.
- [BL1]: Loading BL2 successful.
- [BL1]: Decrypting BL2 successful.
- [BL1]: Authenticating BL2 successful.
- [BL1]: Jumping to BL2...
- [BL2]: Successfully started.

Malicious image

- [BL1]: Successfully started.
- [BL1]: Loading BL2 successful.
- [BL1]: Decrypting BL2 successful.
- [BL1]: Authenticating BL2 unsuccessful. Stopping!

Let's bypass it using fault injection!





LET'S SWITCH TO THE OTHER LAPTOP

OSCILLOSCOPE 1/2

• Pico	Scope 6																						
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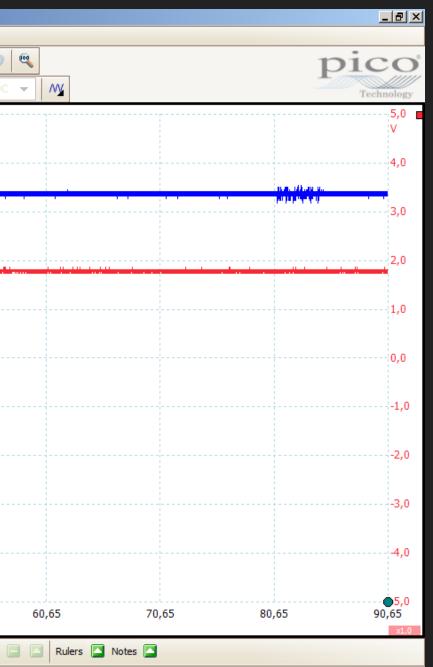
We reset the chip for each experiment.

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OSCILLOSCOPE 2/2

Pico:	Scope 6																				
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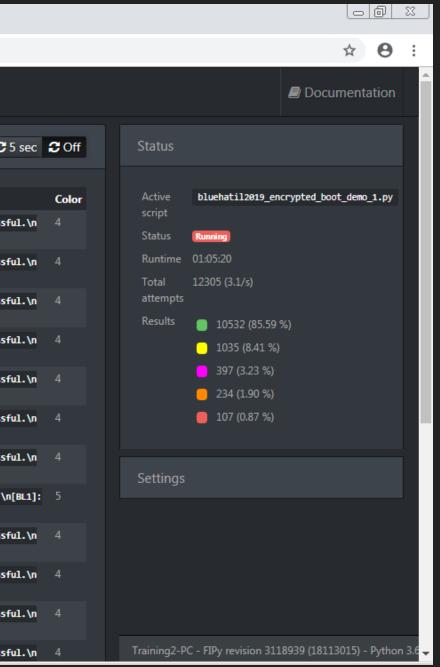
We inject the glitch during the copy of BL2 by BL1.



FIPY 1/3

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	•	12276	44082	1.6512	1405	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
		12275	139318	1.6236	1015	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
	•	12274	197270	2.4543	1227	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
		12273	156778	2.3459	744	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
	•	12272	32745	2.21	1130	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
		12271	190417	1.6173	1496	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
	•	12270	131829	1.7707	1071	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
	•	12269	44625	1.6411	1183	<pre>[BL1]: Successfully started.\n[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\ Decrypting BL2 successful.\n[BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
	•	12268	33465	1.6372	1396	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
		12267	208641	1.9313	1465	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
	-	12266	21400	2.1982	1030	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
		12265	203709	2.1257	1405	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success

Experiments that had no affect on the target are colored green.



FIPY 2/3

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	12877	154309	1.9387	1164			tarted.\n[BL1]: Lo BL2 unsuccesful. 9		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
•	12876	14852	2.0385	960			tarted.\n[BL1]: Lo BL2 unsuccesful. 9		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
•	12875	41274	2.0932	1302			tarted.\n[BL1]: Lo BL2 unsuccesful. 9		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
	12874	248588	1.7791	868	00004\nr3 started.\	3 \t40020800\n	tarted.\nPrinting r12 00000000\nlr \ ng BL2 successful ng.\n	\ t0800 8235\n	pc \t0802afa4\ı	npsr 20000200	<pre>>\n[BL1]: Succes</pre>
•	12873	84387	1.9551	1499			tarted.\n[BL1]: Lo BL2 unsuccesful. !		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
	12872	231344	1.8917	1109			tarted.\n[BL1]: Lo BL2 unsuccesful. S		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
•	12871	165112	2.209	1265			tarted.\n[BL1]: Lo BL2 unsuccesful. S		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
	12870	107311	2.3025	1178			tarted.\n[BL1]: Lo BL2 unsuccesful. S		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
•	12869	228505	2.0327	754			tarted.\n[BL1]: Lo BL2 unsuccesful. 9		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
•	12868	1065	2.1519	1171			tarted.\n[BL1]: Lo BL2 unsuccesful. 9		uccessful.\n[B	L1]: Decrypti	ing BL2 successf
	12867	96109	1.8846	1426	[BL1]: 9	Successfully s	tarted.\n[BL1]: Lo	ading BL2 s	uccessful.\n[B	L1]: Decrypti	ing BL2 successf

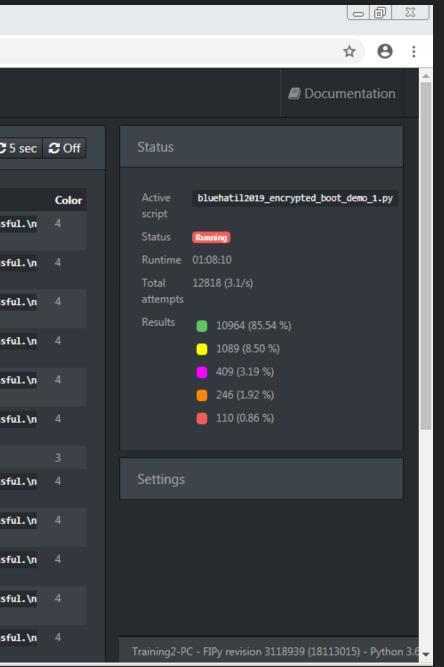
Experiments that resulted in a CPU expection are colored magenta.

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FIPY 3/3

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	•	12773	113607	2.0407	984	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
	•	12772	6099	2.2671	738	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
	•	12771	146840	2.2198	870	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
		12770	233984	1.8955	693	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
	•	12769	219344	2.0889	917	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
	•	12768	222146	1.5007	1283	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
		12767	234484	2.0251	1033	[BL1]: Successfully started.\n\n\nThank you for inviting us!!!!!\n
		12766	133683	1.7813	599	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
	•	12765	181235	1.9552	1220	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
		12764	189253	2.3938	576	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n
	•	12763	50531	1.9885	978	<pre>[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n</pre>
	•	12762	18290	2.092	756	[BL1]: Successfully started.\n[BL1]: Loading BL2 successful.\n[BL1]: Decrypting BL2 success [BL1]: Authenticating BL2 unsuccesful. Stopping.\n

Experiments that resulted in a successful bypass of secure boot are colored red.



WHAT NOW?

WHITE PAPER

"Notes on designing secure boot."

Coming soon!



HARDENING SECURE BOOT

- Keep it simple
- Minimize attacker choices
 - Authenticate everything
 - No weak crypto
- Make software exploitation hard
 - Drop privileges
 - Make fault injection hard
 - Support anti-rollback

WHAT ELSE

SECURE SYSTEM/SW DEVELOPMENT LIFE CYCLE (SECURE SDLC)

- Continuous software review & testing
- Hardware security review & testing

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KEY TAKEAWAYS

- 1. Secure boot is often not optimally hardened
- 2. Attack surface of secure boot is larger than expected
- 3. New perspectives on attacking secure boot

Illy hardened larger than expected secure boot

THANK YOU. QUESTIONS?

riscure

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